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Prepared by: J. L. Odom and D. A. Sheppard	Supersedes None	
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Gamma-ray Large Area Space Telescope (GLAST) Large Area Telescope (LAT) Anti-Coincidence Detector (ACD)

FREE (Front End & Event Electronics)



Comprehensive Performance Test (CPT)

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Document Approval

Prepared by:

James Odom Date
ACD Electronics

Prepared by:

Dave Sheppard Date
ACD Electronics

Approved by:

Glenn Unger Date
ACD Electronics System Lead

Approved by:

George Shibley Date
ACD Systems Engineer

Approved by:

Tom Johnson Date
ACD Project Manager

Approved by:

Dave Thompson Date
ACD Subsystems Manager

Approved by:

Eileen Fowler Date
Quality Assurance

Approved by:

Bob Hartman Date
ACD Scientist

FREE Comprehensive Performance Test

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Document Change Log

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Updated	September 30, 2003	Updates from Review	Jim Odom and Dave Sheppard
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1.0 Scope and Purpose of this Procedure

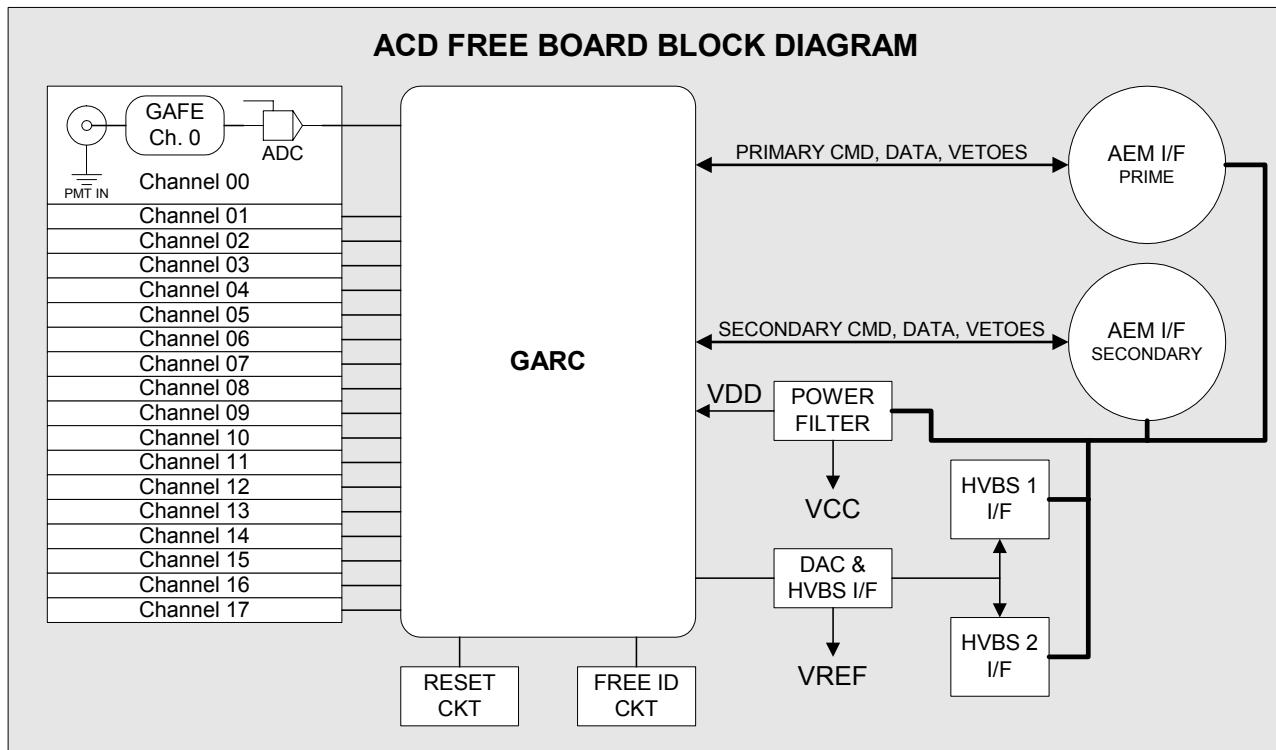
This document describes the instructions for electrical integration of the FREE electronics assembly to the LAT AEM (or AEM GSE) and details the test sequence of the Comprehensive Performance Test (CPT). It does not duplicate all the functions of component-level testing, but instead concentrates on board-level verification issues. This procedure provides the instructions necessary to electrically integrate and functionally test the FREE assembly. This test is intended to be modified to provide other levels of functional testing as required during instrument and spacecraft level integrations.

The FREE assembly is designed to meet the electrical specifications of:

- (1) The ACD Level IV Electronics Requirements, LAT-SS-00352
- (2) The ACD-LAT Interface Control Document, LAT-SS-00-363

2.0 Description of the FREE Electronics Assembly

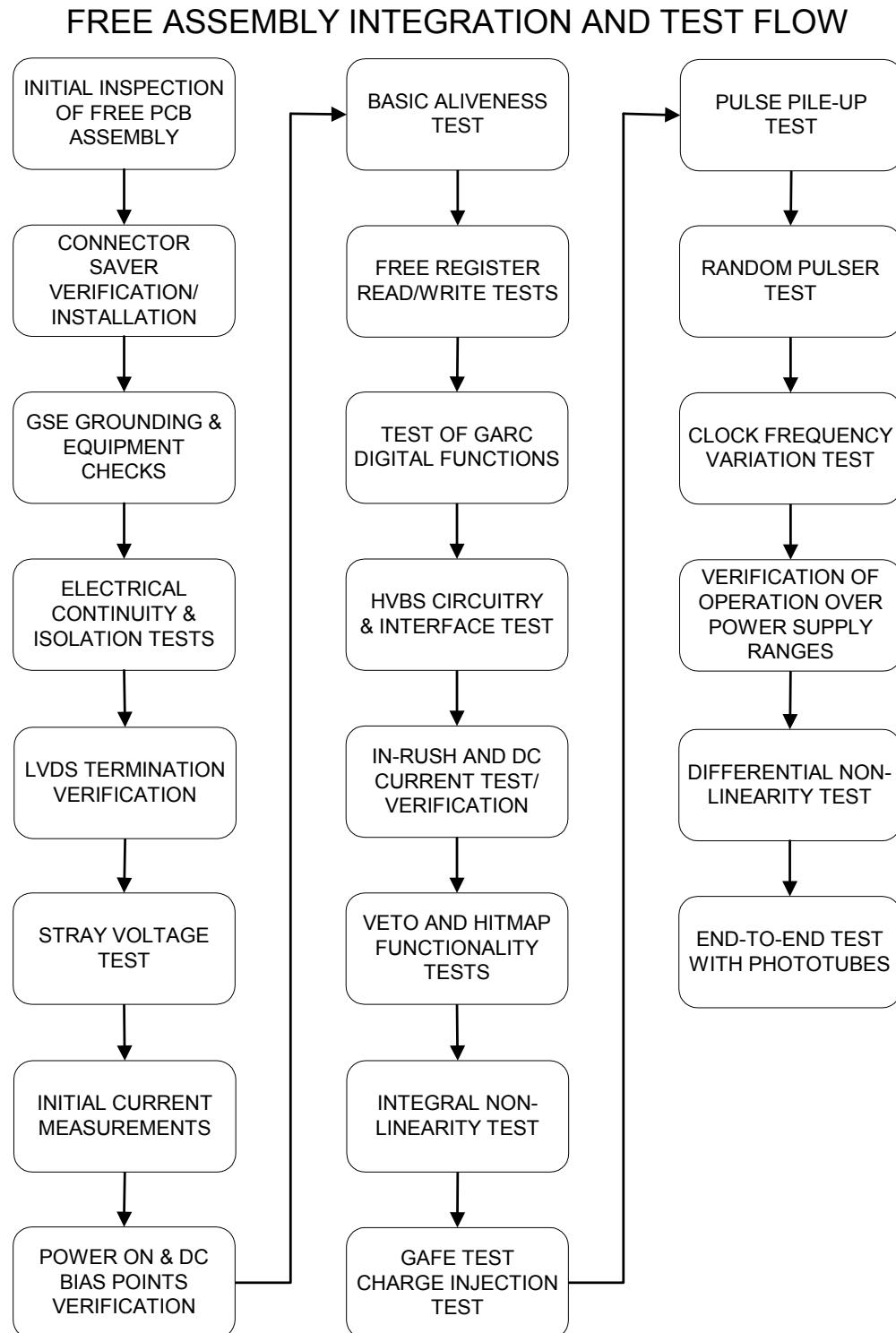
FREE is the acronym for the Gamma-Ray Large Area Space Telescope (GLAST) Anti-Coincidence Detector (ACD) Front End and Event Electronics processing board. The FREE provides the main electrical interface between the ACD and the LAT instrument electronics. The FREE circuitry provides command and data return functions for electronics boards associated with the ACD. There are 12 FREE boards in the flight system, with each FREE card supporting 18 phototube chains and 2 high voltage bias supplies (HVBS). The FREE circuitry utilizes a single +3.3V power supply and provides an interface to pass +28V power to the two HVBS. The FREE is a 10 layer flexible-rigid printed circuit board. It has 18 analog signal processing channels serviced by a single GARC readout controller. It also provides the interface to the HVBS and has two thermistors on board.



The design of the FREE circuitry was done utilizing Orcad for schematic capture, PSpice for simulation, and PADS for board layout. The current copy of the schematic package is posted in PDF format on the ACD website at: <http://lheasoft.gsfc.nasa.gov/acd/electronics/#free>

3.0 Steps of the Electrical Integration and Performance Evaluation

The following block diagram details pictorially the sequence of events required to electrically integrate and test a FREE circuit card assembly with other LAT components.



4.0 Preconditions to and Preparations for Starting this Test

Prior to starting this test, a responsible Test Conductor shall be named. The Test Conductor is responsible for the safety of the hardware and the documentation of results, including anomalies, for the duration of the test. The Test Conductor, or a designated representative, shall be present for each testing sequence. All testing on flight hardware will require a signed Work Authorization Order. Each person working directly with the ACD flight hardware shall be NASA certified for electrostatic discharge control as per NASA-STD-8739.7. All measurement equipment used for verification tests on flight hardware shall have a valid calibration sticker. The Test Conductor shall have the authority to determine deviations from this procedure and shall redline this procedure as necessary. Mates and demates to flight connectors shall be recorded. Connectors shall not be mated nor demated unless the instrument electronics is powered off. Connector savers shall be utilized wherever practical to minimize flight connector mate/demates.

Notify QA 24 hours prior to the start of this test. QA will verify test equipment set up and calibration, review documentation and decide if their presence is required during the testing. Indicate on the test record whether QA was present for the testing.

All measurements and test results will be recorded in the "Test Results Record" Appendix 11. A copy of the entire this entire document is not required each time the test is performed. The appendix will serve as the official record each time this test is performed.

This test will be run at various times during the build-up and Integration of the FREE boards. This test will be run in its entirety during the first turn-on and check-out. If after the successful completion of the initial running of this test the Test Conductor deems that a test should be omitted due to a test point not being accessible or poses a risk to the board the Test Conductor may omit the test by making a note on the Test Record.

4.1 FREE Assembly Identification

The test conductor for this test is: _____

Date of Test: _____

The serial number of the FREE card assembly is: _____

The identification/Serial Number listed on the GARC ASIC is: _____

The identification/Serial Numbers listed on the GAFE ASICs are:

GAFE Channel	ASIC Serial Number
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

10	
11	
12	
13	
14	
15	
16	
17	

Note that for flight assemblies, the performance of this test must be listed on the appropriate Work Authorization Order (WOA).

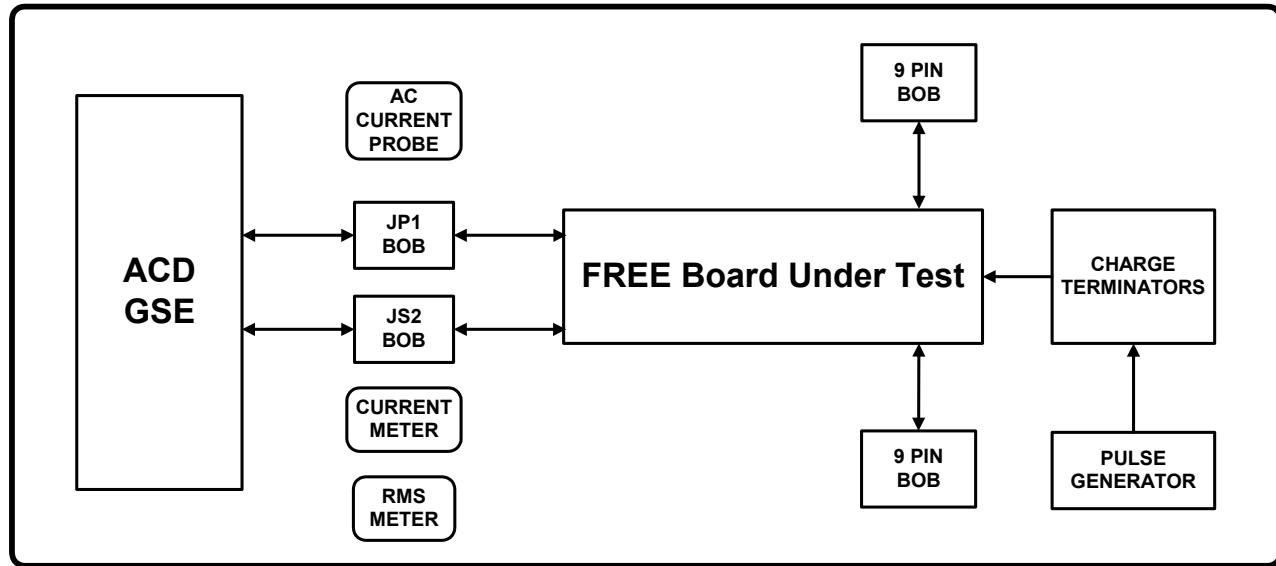
4.2 Test Equipment Utilized

Prior to starting this test, the Test Conductor shall record the test and measurement hardware used in the performance of this test. Note that all multimeters used in testing of the FREE circuit card assembly shall be of low current output design, such as the Fluke 70 series, HP3400 series or similar. High current output multimeters are not compatible with the FREE circuitry.

Instrument Type	Manufacturer & Model Number	NASA ID Number	Calibration Due Date
Power Supply for HVBS +28V			
Power Supply for FREE & GSE +3.3V & +5.0V			
Multimeter 1			
Multimeter 2			
Tail Pulse Generator			
Oscilloscope			
AC Current Probe			
RMS Voltmeter			
Pulse Generator			
Charge Terminator Box			

4.3 Suggested Equipment Setup

Prior to starting the test, it is recommended that the laboratory bench be set up as follows:



4.4 Verification of the GSE Ground

Prior to the connection of FREE assembly hardware to other electronics, it shall be verified that all power supplies, signal generators, VME racks, and any other test and measurement equipment shall be connected to the same AC ground. The simplest way to do this is to connect all AC-powered equipment to the same power strip. In cases where this is not practical (e.g., possibly a thermal-vacuum test), greater care must be taken to ensure there are no floating grounds since this would represent a hazard to the FREE assembly.

4.5 Description of the ACD Interface Signals

ACD_CLK: Nominal 20 MHz \pm 1% continuous, 45-55% duty cycle clock from the ACD Electronics Module (AEM). This clock can be tested outside this range.

ACD_NSCMD: The command signal from AEM. The ACD_NSCMD signal transitions on the trailing edge of ACD_CLK and is shifted into the ACD on the leading edge of ACD_CLK. A single start bit, (logic 1), signals the beginning of a command.

ACD_NRST: Reset from AEM. ACD_NRST is synchronous to ACD_CLK. ACD_NRST at logic one resets state machines and initializes registers and modes in ACD. The ACD_NRST is at least five ACD_CLK cycles.

ACD_NS DATA: Data from ACD. The ACD_NS DATA signal transitions on the leading edge of ACD_CLK. The beginning of a data packet indicated by a single start bit.

ACD_NCNO: The ACD_NCNO interface signal is the OR of the selected (via command) HLD discriminators.

ACD_NVETOs: Veto discriminator output signals from ACD.

ACD_HV: Analog monitor of the high voltage power supply voltage output. 0 - 2.5 volts indicates 0 - full-scale volts at the supply output. Pseudo differential analog, with signal on ACD_HVP and ground on ACD_HVN, $10\text{K} \pm 5\%$ source impedance all lines.

ACD_TEMP: ACD board temperature monitor, 30K thermistor, GSFC S-311-P-18 series (YSI 44900 series).

ACD_VDD(0-2): +3.3V supplied by the AEM to the ACD FREE circuit cards.

ACD_28V(0-1): +28V supplied by the AEM to the ACD HVBSs.

5.0 Electrical Safe-to-Mate Verification of the FREE Assembly

The intent of this section is to ensure that the FREE assembly is both electrically and mechanically safe to mate to the AEM or AEM GSE to be used for testing.

Break Out Boxes (BOB) and a calibrated multimeter will be required for this test.

This section is to be performed prior to doing electrical testing on the FREE assembly. If this verification has been performed successfully, the Test Conductor may opt to omit this portion of the test if both the FREE assembly and the AEM interface have been checked.

1. Verify that connector savers have been installed on FREE connectors JP1, JS2, JHV1, and JHV2.
2. Verify that break out boxes (BOB) are available for these four connectors. These BOB should have been pin-for-pin checked for continuity and isolation prior to the start of this procedure.
3. The test conductor shall visually inspect each of the connector halves on the FREE assembly, BOB, harnessing, and AEM interface to ensure there are no bent pins, debris, or other physical damage that would impede safe connector mating.
4. All shorting pins should be removed from the BOBs.
5. Verify that the power supplies are OFF.
6. Mate the four BOBs to connectors JP1, JS2, JHV1 and JHV2 on the FREE assembly. Mate the other side of the BOBs to the AEM interface connectors.

5.1 Electrical Continuity Check

With the shorting plugs removed from the break out box, make the following continuity measurements on the FREE assembly side of the interface.

This test may be omitted at the discretion of the Test Conductor.

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_VDD	JP1 - 3	JP1 - 1	R < 1 Ω	
2	ACD_VDD	JP1 - 4	JP1 - 1	R < 1 Ω	
3	ACD_VDD	JS2 - 1	JP1 - 1	R < 1 Ω	
4	ACD_VDD	JS2 - 3	JP1 - 1	R < 1 Ω	
5	ACD_VDD	JS2 - 4	JP1 - 1	R < 1 Ω	
6	ACD_RTN	JP1-31	JP1-30	R < 1 Ω	
7	ACD_RTN	JP1-32	JP1-30	R < 1 Ω	
8	ACD_RTN	JS2-30	JP1-30	R < 1 Ω	
9	ACD_RTN	JS2-31	JP1-30	R < 1 Ω	
10	ACD_RTN	JS2-32	JP1-30	R < 1 Ω	
11	ACD_28V	JP1-7	JP1-5	R < 1 Ω	
12	ACD_28V	JS2-5	JP1-5	R < 1 Ω	
13	ACD_28V	JS2-7	JP1-5	R < 1 Ω	
14	ACD_28V	JHV1-1	JP1-5	R < 1 Ω	
15	ACD_28V	JHV1-6	JP1-5	R < 1 Ω	
16	ACD_28V	JHV2-1	JP1-5	R < 1 Ω	
17	ACD_28V	JHV2-6	JP1-5	R < 1 Ω	
18	ACD_28V_RTN	JP1-34	JP1-33	R < 1 Ω	
19	ACD_28V_RTN	JS2-33	JP1-33	R < 1 Ω	
20	ACD_28V_RTN	JS2-34	JP1-33	R < 1 Ω	
21	ACD_28V_RTN	JHV1-2	JP1-33	R < 1 Ω	

22	ACD_28V_RTN	JHV1-7	JP1-33	R < 1 Ω	
23	ACD_28V_RTN	JHV2-2	JP1-33	R < 1 Ω	
24	ACD_28V_RTN	JHV2-7	JP1-33	R < 1 Ω	
25	HV_DACP	JHV1-4	JHV2-4	R < 1 Ω	
26	HV_DACN	JHV1-9	JHV2-9	R < 1 Ω	
27	HV1_MONP	JHV1-3	JP1-23	R < 1 Ω	
28	HV1_MONP	JHV1-3	JS2-23	R < 1 Ω	
29	HV1_MONN	JHV1-8	JP1-24	R < 1 Ω	
30	HV1_MONN	JHV1-8	JS2-24	R < 1 Ω	
31	HV2_MONP	JHV2-3	JP1-27	R < 1 Ω	
32	HV2_MONP	JHV2-3	JS2-27	R < 1 Ω	
33	HV2_MONN	JHV2-8	JP1-28	R < 1 Ω	
34	HV2_MONN	JHV2-8	JS2-28	R < 1 Ω	

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

5.2 Electrical Isolation Check

With the shorting plugs removed from the break out box, make the following isolation measurements on the FREE assembly side of the interface.

This test may be omitted at the discretion of the Test Conductor.

Meas. No.	Signal 1	Signal 2	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_VDD	ACD_RTN	JP1 - 1	JP1 - 30	R > 1 kΩ	
2	ACD_VDD	ACD_28V	JP1 - 1	JP1 - 5	R > 1 MΩ	
3	ACD_VDD	ACD_28V_RTN	JP1 - 1	JP1 - 33	R > 1 MΩ	
4	ACD_28V	ACD_RTN	JP1 - 5	JP1 - 30	R > 1 MΩ	
5	ACD_28V	ACD_28V_RTN	JP1 - 5	JP1 - 33	R > 1 kΩ	
6	ACD_RTN	ACD_28V_RTN	JS2 - 30	JP1 - 33	R > 90 Ω	
7	ACD_NVETO_00AP	ACD_NVETO_00AM	JP1-70	JP1-71	R > 40 kΩ	
8	ACD_NVETO_01AP	ACD_NVETO_01AM	JP1-68	JP1-69	R > 40 kΩ	
9	ACD_NVETO_02AP	ACD_NVETO_02AM	JP1-66	JP1-67	R > 40 kΩ	
10	ACD_NVETO_03AP	ACD_NVETO_03AM	JP1-64	JP1-65	R > 40 kΩ	
11	ACD_NVETO_04AP	ACD_NVETO_04AM	JP1-62	JP1-63	R > 40 kΩ	
12	ACD_NVETO_05AP	ACD_NVETO_05AM	JP1-60	JP1-61	R > 40 kΩ	
13	ACD_NVETO_06AP	ACD_NVETO_06AM	JP1-58	JP1-59	R > 40 kΩ	
14	ACD_NVETO_07AP	ACD_NVETO_07AM	JP1-56	JP1-57	R > 40 kΩ	
15	ACD_NVETO_08AP	ACD_NVETO_08AM	JP1-54	JP1-55	R > 40 kΩ	
16	ACD_NVETO_09AP	ACD_NVETO_09AM	JP1-52	JP1-53	R > 40 kΩ	
17	ACD_NVETO_10AP	ACD_NVETO_10AM	JP1-50	JP1-51	R > 40 kΩ	
18	ACD_NVETO_11AP	ACD_NVETO_11AM	JP1-48	JP1-49	R > 40 kΩ	
19	ACD_NVETO_12AP	ACD_NVETO_12AM	JP1-46	JP1-47	R > 40 kΩ	
20	ACD_NVETO_13AP	ACD_NVETO_13AM	JP1-44	JP1-45	R > 40 kΩ	
21	ACD_NVETO_14AP	ACD_NVETO_14AM	JP1-42	JP1-43	R > 40 kΩ	
22	ACD_NVETO_15AP	ACD_NVETO_15AM	JP1-40	JP1-41	R > 40 kΩ	
23	ACD_NVETO_16AP	ACD_NVETO_16AM	JP1-17	JP1-18	R > 40 kΩ	
24	ACD_NVETO_17AP	ACD_NVETO_17AM	JP1-19	JP1-20	R > 40 kΩ	
25	ACD_NCNO_AP	ACD_NCNO_AM	JP1-21	JP1-22	R > 40 kΩ	
26	ACD_NSDATA_AP	ACD_NSDATA_AM	JP1-72	JP1-73	R > 40 kΩ	

27	ACD_NRST_AP	ACD_NTST_AM	JP1-74	JP1-75	95 Ω < R < 105 Ω	
28	ACD_NSCMD_AP	ACD_NSCMD_AM	JP1-76	JP1-77	95 Ω < R < 105 Ω	
29	ACD_NSCLK_AP	ACD_NSCLK_AM	JP1-78	JP1-79	95 Ω < R < 105 Ω	
30	ACD_HV_AP	ACD_HV_AM	JP1-23	JP1-24	R > 100 kΩ	
31	ACD_TEMP_AP	ACD_TEMP_AM	JP1-25	JP1-26	R > 20 kΩ	
32	ACD_NVETO_00BP	ACD_NVETO_00BM	JS2-70	JS2-71	R > 40 kΩ	
33	ACD_NVETO_01BP	ACD_NVETO_01BM	JS2-68	JS2-69	R > 40 kΩ	
34	ACD_NVETO_02BP	ACD_NVETO_02BM	JS2-66	JS2-67	R > 40 kΩ	
35	ACD_NVETO_03BP	ACD_NVETO_03BM	JS2-64	JS2-65	R > 40 kΩ	
36	ACD_NVETO_04BP	ACD_NVETO_04BM	JS2-62	JS2-63	R > 40 kΩ	
37	ACD_NVETO_05BP	ACD_NVETO_05BM	JS2-60	JS2-61	R > 40 kΩ	
38	ACD_NVETO_06BP	ACD_NVETO_06BM	JS2-58	JS2-59	R > 40 kΩ	
39	ACD_NVETO_07BP	ACD_NVETO_07BM	JS2-56	JS2-57	R > 40 kΩ	
40	ACD_NVETO_08BP	ACD_NVETO_08BM	JS2-54	JS2-55	R > 40 kΩ	
41	ACD_NVETO_09BP	ACD_NVETO_09BM	JS2-52	JS2-53	R > 40 kΩ	
42	ACD_NVETO_10BP	ACD_NVETO_10BM	JS2-50	JS2-51	R > 40 kΩ	
43	ACD_NVETO_11BP	ACD_NVETO_11BM	JS2-48	JS2-49	R > 40 kΩ	
44	ACD_NVETO_12BP	ACD_NVETO_12BM	JS2-46	JS2-47	R > 40 kΩ	
45	ACD_NVETO_13BP	ACD_NVETO_13BM	JS2-44	JS2-45	R > 40 kΩ	
46	ACD_NVETO_14BP	ACD_NVETO_14BM	JS2-42	JS2-43	R > 40 kΩ	
47	ACD_NVETO_15BP	ACD_NVETO_15BM	JS2-40	JS2-41	R > 40 kΩ	
48	ACD_NVETO_16BP	ACD_NVETO_16BM	JS2-17	JS2-18	R > 40 kΩ	
49	ACD_NVETO_17BP	ACD_NVETO_17BM	JS2-19	JS2-20	R > 40 kΩ	
50	ACD_NCNO_BP	ACD_NCNO_BM	JS2-21	JS2-22	R > 40 kΩ	
51	ACD_NSDATA_BP	ACD_NSDATA_BM	JS2-72	JS2-73	R > 40 kΩ	
52	ACD_NRST_BP	ACD_NTST_BM	JS2-74	JS2-75	95 Ω < R < 105 Ω	
53	ACD_NSCMD_BP	ACD_NSCMD_BM	JS2-76	JS2-77	95 Ω < R < 105 Ω	
54	ACD_NSCLK_BP	ACD_NSCLK_BM	JS2-78	JS2-79	95 Ω < R < 105 Ω	
55	ACD_HV_BP	ACD_HV_BM	JS2-23	JS2-24	R > 100 kΩ	
56	ACD_TEMP_BP	ACD_TEMP_BM	JS2-25	JS2-26	R > 20 kΩ	

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

5.3 Verification of Proper LVDS Terminations

The ACD interface requires proper termination of the LVDS drivers. The specification is $100 \Omega \pm 5\%$. This test is performed with the ACD power off. A multimeter is used to measure the impedance across the following signal pairs on the GSE side of the BOB and the result is recorded

This test may be omitted at the discretion of the Test Conductor.

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_NVETO_16_A	JP1 - 17	JP1 - 18	95 Ω < R < 105 Ω	
2	ACD_NVETO_17_A	JP1 - 19	JP1 - 20	95 Ω < R < 105 Ω	
3	ACD_CNO_A	JP1 - 21	JP1 - 22	95 Ω < R < 105 Ω	
4	ACD_NVETO_15_A	JP1 - 40	JP1 - 41	95 Ω < R < 105 Ω	
5	ACD_NVETO_14_A	JP1 - 42	JP1 - 43	95 Ω < R < 105 Ω	
6	ACD_NVETO_13_A	JP1 - 44	JP1 - 45	95 Ω < R < 105 Ω	
7	ACD_NVETO_12_A	JP1 - 46	JP1 - 47	95 Ω < R < 105 Ω	
8	ACD_NVETO_11_A	JP1 - 48	JP1 - 49	95 Ω < R < 105 Ω	

9	ACD_NVETO_10_A	JP1 - 50	JP1 - 51	95 Ω < R < 105 Ω	
10	ACD_NVETO_09_A	JP1 - 52	JP1 - 53	95 Ω < R < 105 Ω	
11	ACD_NVETO_08_A	JP1 - 54	JP1 - 55	95 Ω < R < 105 Ω	
12	ACD_NVETO_07_A	JP1 - 56	JP1 - 57	95 Ω < R < 105 Ω	
13	ACD_NVETO_06_A	JP1 - 58	JP1 - 59	95 Ω < R < 105 Ω	
14	ACD_NVETO_05_A	JP1 - 60	JP1 - 61	95 Ω < R < 105 Ω	
15	ACD_NVETO_04_A	JP1 - 62	JP1 - 63	95 Ω < R < 105 Ω	
16	ACD_NVETO_03_A	JP1 - 64	JP1 - 65	95 Ω < R < 105 Ω	
17	ACD_NVETO_02_A	JP1 - 66	JP1 - 67	95 Ω < R < 105 Ω	
18	ACD_NVETO_01_A	JP1 - 68	JP1 - 69	95 Ω < R < 105 Ω	
19	ACD_NVETO_00_A	JP1 - 70	JP1 - 71	95 Ω < R < 105 Ω	
20	ACD_NSDATA_A	JP1 - 72	JP1 - 73	95 Ω < R < 105 Ω	
21	ACD_NRST_A	JP1 - 74	JP1 - 75	R > 100 kΩ	
22	ACD_NSCMD_A	JP1 - 76	JP1 - 77	R > 100 kΩ	
23	ACD_CLK_A	JP1 - 78	JP1 - 79	R > 100 kΩ	
24	ACD_NVETO_16_B	JS2 - 17	JS2 - 18	95 Ω < R < 105 Ω	
25	ACD_NVETO_17_B	JS2 - 19	JS2 - 20	95 Ω < R < 105 Ω	
26	ACD_CNO_B	JS2 - 21	JS2 - 22	95 Ω < R < 105 Ω	
27	ACD_NVETO_15_B	JS2 - 40	JS2 - 41	95 Ω < R < 105 Ω	
28	ACD_NVETO_14_B	JS2 - 42	JS2 - 43	95 Ω < R < 105 Ω	
29	ACD_NVETO_13_B	JS2 - 44	JS2 - 45	95 Ω < R < 105 Ω	
30	ACD_NVETO_12_B	JS2 - 46	JS2 - 47	95 Ω < R < 105 Ω	
31	ACD_NVETO_11_B	JS2 - 48	JS2 - 49	95 Ω < R < 105 Ω	
32	ACD_NVETO_10_B	JS2 - 50	JS2 - 51	95 Ω < R < 105 Ω	
33	ACD_NVETO_09_B	JS2 - 52	JS2 - 53	95 Ω < R < 105 Ω	
34	ACD_NVETO_08_B	JS2 - 54	JS2 - 55	95 Ω < R < 105 Ω	
35	ACD_NVETO_07_B	JS2 - 56	JS2 - 57	95 Ω < R < 105 Ω	
36	ACD_NVETO_06_B	JS2 - 58	JS2 - 59	95 Ω < R < 105 Ω	
37	ACD_NVETO_05_B	JS2 - 60	JS2 - 61	95 Ω < R < 105 Ω	
38	ACD_NVETO_04_B	JS2 - 62	JS2 - 63	95 Ω < R < 105 Ω	
39	ACD_NVETO_03_B	JS2 - 64	JS2 - 65	95 Ω < R < 105 Ω	
40	ACD_NVETO_02_B	JS2 - 66	JS2 - 67	95 Ω < R < 105 Ω	
41	ACD_NVETO_01_B	JS2 - 68	JS2 - 69	95 Ω < R < 105 Ω	
42	ACD_NVETO_00_B	JS2 - 70	JS2 - 71	95 Ω < R < 105 Ω	
43	ACD_NSDATA_B	JS2 - 72	JS2 - 73	95 Ω < R < 105 Ω	
44	ACD_NRST_B	JS2 - 74	JS2 - 75	R > 100 kΩ	
45	ACD_NSCMD_B	JS2 - 76	JS2 - 77	R > 100 kΩ	
46	ACD_CLK_B	JS2 - 78	JS2 - 79	R > 100 kΩ	

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

6.0 Initial Power-On Measurements

With the shorting plugs removed from the break out boxes, turn the ACD power on and perform the following voltage measurements.

This section is to be performed prior to doing electrical testing on the FREE assembly. If this verification has been performed successfully, the Test Conductor may opt to omit this portion of the test if the AEM interface has been checked.

6.1 Stray Voltage Test at the AEM Interface

With the shorting plugs removed from the break out boxes, turn the ACD power on and perform the following voltage measurements on the AEM interface side of the break out box. The (-) input to the voltmeter may be referenced to pin 30, the +3.3V return.

This test may be omitted at the discretion of the Test Conductor.

Meas. No.	AEM Interface Pin	Signal Name	Expected Voltage	Measured Voltage
1	JP1 - 1	ACD_VDD_0A	+3.3V	
2	JP1 - 3	ACD_VDD_1A	+3.3V	
3	JP1 - 4	ACD_VDD_2A	+3.3V	
4	JP1 - 5	ACD_28V_0A	+28V	
5	JP1 - 7	ACD_28V_1A	+28V	
6	JP1 - 17	ACD_NVETO_16AP	0< V < 3.3	
7	JP1 - 18	ACD_NVETO_16AM	0< V < 3.3	
8	JP1 - 19	ACD_NVETO_17AP	0< V < 3.3	
9	JP1 - 20	ACD_NVETO_17AM	0< V < 3.3	
10	JP1 - 21	ACD_NCNO_AP	0< V < 3.3	
11	JP1 - 22	ACD_NCNO_AM	0< V < 3.3	
12	JP1 - 23	ACD_HV_AP	0< V < 3.3	
13	JP1 - 24	ACD_HV_AM	0< V < 3.3	
14	JP1 - 25	ACD_TEMP_AP	TBD	
15	JP1 - 26	ACD_TEMP_AM	TBD	
16	JP1 - 30	ACD_GND_0A	0	
17	JP1 - 31	ACD_GND_1A	0	
18	JP1 - 32	ACD_GND_2A	0	
19	JP1 - 33	ACD_28V_RTN_0A	0	
20	JP1 - 34	ACD_28V_RTN_1A	0	
21	JP1 - 40	ACD_NVETO_15AM	V < 200mV	
22	JP1 - 41	ACD_NVETO_15AP	V < 200mV	
23	JP1 - 42	ACD_NVETO_14AM	V < 200mV	
24	JP1 - 43	ACD_NVETO_14AP	V < 200mV	
25	JP1 - 44	ACD_NVETO_13AM	V < 200mV	
26	JP1 - 45	ACD_NVETO_13AP	V < 200mV	
27	JP1 - 46	ACD_NVETO_12AM	V < 200mV	
28	JP1 - 47	ACD_NVETO_12AP	V < 200mV	
29	JP1 - 48	ACD_NVETO_11AM	V < 200mV	
31	JP1 - 50	ACD_NVETO_10AM	V < 200mV	
32	JP1 - 51	ACD_NVETO_10AP	V < 200mV	
33	JP1 - 52	ACD_NVETO_09AM	V < 200mV	

34	JP1 - 53	ACD_NVETO_09AP	V < 200mV
35	JP1 - 54	ACD_NVETO_08AM	V < 200mV
36	JP1 - 55	ACD_NVETO_08AP	V < 200mV
37	JP1 - 56	ACD_NVETO_07AM	V < 200mV
38	JP1 - 57	ACD_NVETO_07AP	V < 200mV
39	JP1 - 58	ACD_NVETO_06AM	V < 200mV
40	JP1 - 59	ACD_NVETO_06AP	V < 200mV
41	JP1 - 60	ACD_NVETO_05AM	V < 200mV
42	JP1 - 61	ACD_NVETO_05AP	V < 200mV
43	JP1 - 62	ACD_NVETO_04AM	V < 200mV
44	JP1 - 63	ACD_NVETO_04AP	V < 200mV
45	JP1 - 64	ACD_NVETO_03AM	V < 200mV
46	JP1 - 65	ACD_NVETO_03AP	V < 200mV
47	JP1 - 66	ACD_NVETO_02AM	V < 200mV
48	JP1 - 67	ACD_NVETO_02AP	V < 200mV
49	JP1 - 68	ACD_NVETO_01AM	V < 200mV
50	JP1 - 69	ACD_NVETO_01AP	V < 200mV
51	JP1 - 70	ACD_NVETO_00AM	V < 200mV
52	JP1 - 71	ACD_NVETO_00AP	V < 200mV
53	JP1 - 72	ACD_NS DATA_AM	V < 200mV
54	JP1 - 73	ACD_NS DATA_AP	V < 200mV
55	JP1 - 74	ACD_NRST_AM	V < 200mV
56	JP1 - 75	ACD_NRST_AP	V > 2.3V
57	JP1 - 76	ACD_NSCMD_AM	V < 200mV
58	JP1 - 77	ACD_NSCMD_AP	V > 2.3V
59	JP1 - 78	ACD_CLK_AM	1.1V < V < 1.5V
60	JP1 - 79	ACD_CLK_AP	1.1V < V < 1.5V
61	JS2 - 1	ACD_VDD_0B	+3.3V
62	JS2 - 3	ACD_VDD_1B	+3.3V
63	JS2 - 4	ACD_VDD_2B	+3.3V
64	JS2 - 5	ACD_28V_0B	+28V
65	JS2 - 7	ACD_28V_1B	+28V
66	JS2 - 17	ACD_NVETO_16BP	V < 200mV
67	JS2 - 18	ACD_NVETO_16BM	V < 200mV
68	JS2 - 19	ACD_NVETO_17BP	V < 200mV
69	JS2 - 20	ACD_NVETO_17BM	V < 200mV
70	JS2 - 21	ACD_NCNO_BP	V < 200mV
71	JS2 - 22	ACD_NCNO_BM	V < 200mV
72	JS2 - 23	ACD_HV_BP	V < 200mV
73	JS2 - 24	ACD_HV_BM	V < 200mV
74	JS2 - 25	ACD_TEMP_BP	TBD
75	JS2 - 26	ACD_TEMP_BM	TBD
76	JS2 - 30	ACD_GND_0B	0
77	JS2 - 31	ACD_GND_1B	0
78	JS2 - 32	ACD_GND_2B	0
79	JS2 - 33	ACD_28V_RTN_0B	0
80	JS2 - 34	ACD_28V_RTN_1B	0
81	JS2 - 40	ACD_NVETO_15BM	V < 200mV
82	JS2 - 41	ACD_NVETO_15BP	V < 200mV
83	JS2 - 42	ACD_NVETO_14BM	V < 200mV
84	JS2 - 43	ACD_NVETO_14BP	V < 200mV

85	JS2 - 44	ACD_NVETO_13BM	V < 200mV
86	JS2 - 45	ACD_NVETO_13BP	V < 200mV
87	JS2 - 46	ACD_NVETO_12BM	V < 200mV
88	JS2 - 47	ACD_NVETO_12BP	V < 200mV
89	JS2 - 48	ACD_NVETO_11BM	V < 200mV
90	JS2 - 49	ACD_NVETO_11BP	V < 200mV
91	JS2 - 50	ACD_NVETO_10BM	V < 200mV
92	JS2 - 51	ACD_NVETO_10BP	V < 200mV
93	JS2 - 52	ACD_NVETO_09BM	V < 200mV
94	JS2 - 53	ACD_NVETO_09BP	V < 200mV
95	JS2 - 54	ACD_NVETO_08BM	V < 200mV
96	JS2 - 55	ACD_NVETO_08BP	V < 200mV
97	JS2 - 56	ACD_NVETO_07BM	V < 200mV
98	JS2 - 57	ACD_NVETO_07BP	V < 200mV
99	JS2 - 58	ACD_NVETO_06BM	V < 200mV
100	JS2 - 59	ACD_NVETO_06BP	V < 200mV
101	JS2 - 60	ACD_NVETO_05BM	V < 200mV
102	JS2 - 61	ACD_NVETO_05BP	V < 200mV
103	JS2 - 62	ACD_NVETO_04BM	V < 200mV
104	JS2 - 63	ACD_NVETO_04BP	V < 200mV
105	JS2 - 64	ACD_NVETO_03BM	V < 200mV
106	JS2 - 65	ACD_NVETO_03BP	V < 200mV
107	JS2 - 66	ACD_NVETO_02BM	V < 200mV
108	JS2 - 67	ACD_NVETO_02BP	V < 200mV
109	JS2 - 68	ACD_NVETO_01BM	V < 200mV
110	JS2 - 69	ACD_NVETO_01BP	V < 200mV
111	JS2 - 70	ACD_NVETO_00BM	V < 200mV
112	JS2 - 71	ACD_NVETO_00BP	V < 200mV
113	JS2 - 72	ACD_NSDATA_BM	V < 200mV
114	JS2 - 73	ACD_NSDATA_BP	V < 200mV
115	JS2 - 74	ACD_NRST_BM	V < 200mV
116	JS2 - 75	ACD_NRST_BP	V > 2.3V
117	JS2 - 76	ACD_NSCMD_BM	V < 200mV
118	JS2 - 77	ACD_NSCMD_BP	V > 2.3V
119	JS2 - 78	ACD_CLK_BM	1.1V < V < 1.5V
120	JS2 - 79	ACD_CLK_BP	1.1V < V < 1.5V

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

6.2 Electrical Integration of the FREE Card and Initial Current Tests

The pin connections for the two 79 pin circular connectors JP1 and JS2 are listed in Appendix 7. The pin connections for the two 9 pin MDM connectors to the High Voltage Bias Supplies are listed in Appendix 6.

At this time, insert all jumper plugs into the break out boxes on connectors JP1, JS2. Please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

6.3 Measurement of the Power Supply, DC Bias and Reference Voltages

This section measures DC voltages at several points on the FREE board and compares them to the expected values. Using the digital multimeter (autoscaling) and measuring DC volts, connect the (-) lead to one of the LepraCon connector shells and measure the following voltages with the (+) lead at the FREE board location listed in the table below.

Turn on the +3.3V and +28V supplies and record the currents below or in the Test Record associated with this procedure.

+3.3V Current - _____

+28V Current - _____

This portion of the test may be omitted at the discretion of the Test Conductor.

Meas. No.	FREE Circuit Card Probe Point	Alternate Probe Point	Expected Voltage	Measured Voltage
1	UADC00-5	CA4-1	2.50 V	
2	UADC01-5	C139-1	2.50 V	
3	UADC02-5	C172-1	2.50 V	
4	UADC03-5	C183-1	2.50 V	
5	UADC04-5	C29-1	2.50 V	
6	UADC05-5	C40-1	2.50 V	
7	UADC06-5	C73-1	2.50 V	
8	UADC07-5	C84-1	2.50 V	
9	UADC08-5	C117-1	2.50 V	
10	UADC09-5	C128-1	2.50 V	
11	UADC10-5	C150-1	2.50 V	
12	UADC11-5	C161-1	2.50 V	
13	UADC12-5	C194-1	2.50 V	
14	UADC13-5	C208-1	2.50 V	
15	UADC14-5	C51-1	2.50 V	
16	UADC15-5	C62-1	2.50 V	
17	UADC16-5	C95-1	2.50 V	
18	UADC17-5	C106-1	2.50 V	
19	UGA00-8	C266-1	2.50 V	
20	UGA01-8	C248-1	2.50 V	
21	UGA02-8	C257-1	2.50 V	
22	UGA03-8	C260-1	2.50 V	
23	UGA04-8	C218-1	2.50 V	
24	UGA05-8	C221-1	2.50 V	
25	UGA06-8	C230-1	2.50 V	
26	UGA07-8	C233-1	2.50 V	
27	UGA08-8	C242-1	2.50 V	
28	UGA09-8	C245-1	2.50 V	
29	UGA10-8	C251-1	2.50 V	
30	UGA11-8	C254-1	2.50 V	
31	UGA12-8	C263-1	2.50 V	
32	UGA13-8	C269-1	2.50 V	
33	UGA14-8	C224-1	2.50 V	
34	UGA15-8	C227-1	2.50 V	
35	UGA16-8	C236-1	2.50 V	

36	UGA17-8	C239-1	2.50 V	
37	UGA00-22 (VDD)	CA5-1	> 3.1 V	
38	UGA01-22 (VDD)	CA5-1	> 3.1 V	
39	UGA02-22 (VDD)	C143-1	> 3.1 V	
40	UGA03-22 (VDD)	C176-1	> 3.1 V	
41	UGA04-22 (VDD)	C33-1	> 3.1 V	
42	UGA05-22 (VDD)	C44-1	> 3.1 V	
43	UGA06-22 (VDD)	C77-1	> 3.1 V	
44	UGA07-22 (VDD)	C88-1	> 3.1 V	
45	UGA08-22 (VDD)	C121-1	> 3.1 V	
46	UGA09-22 (VDD)	C132-1	> 3.1 V	
47	UGA10-22 (VDD)	C154-1	> 3.1 V	
48	UGA11-22 (VDD)	C165-1	> 3.1 V	
49	UGA12-22 (VDD)	C198-1	> 3.1 V	
50	UGA13-22 (VDD)	C212-1	> 3.1 V	
51	UGA14-22 (VDD)	C55-1	> 3.1 V	
52	UGA15-22 (VDD)	C66-1	> 3.1 V	
53	UGA16-22 (VDD)	C99-1	> 3.1 V	
54	UGA17-22 (VDD)	C110-1	> 3.1 V	
55	UGA00-1 (VCC)	CA7-1	> 3.1 V	
56	UGA01-1 (VCC)	C145-1	> 3.1 V	
57	UGA02-1 (VCC)	C178-1	> 3.1 V	
58	UGA03-1 (VCC)	C189-1	> 3.1 V	
59	UGA04-1 (VCC)	C35-1	> 3.1 V	
60	UGA05-1 (VCC)	C46-1	> 3.1 V	
61	UGA06-1 (VCC)	C79-1	> 3.1 V	
62	UGA07-1 (VCC)	C90-1	> 3.1 V	
63	UGA08-1 (VCC)	C123-1	> 3.1 V	
64	UGA09-1 (VCC)	C134-1	> 3.1 V	
65	UGA10-1 (VCC)	C156-1	> 3.1 V	
66	UGA11-1 (VCC)	C167-1	> 3.1 V	
67	UGA12-1 (VCC)	C200-1	> 3.1 V	
68	UGA13-1 (VCC)	C214-1	> 3.1 V	
69	UGA14-1 (VCC)	C57-1	> 3.1 V	
70	UGA15-1 (VCC)	C68-1	> 3.1 V	
71	UGA16-1 (VCC)	C101-1	> 3.1 V	
72	UGA17-1 (VCC)	C112-1	> 3.1 V	
73	TPR1	UR1-2	< 0.2 V	
74	DR1-A	UR1-1	> 3.0 V	
75	UID1-1	N/A	< 0.2 V	
76	UID1-2	N/A	< 0.2 V	
77	UID1-3	N/A	N/A (ID_4)	
78	UID1-4	N/A	N/A (ID_5)	
79	UID1-5	N/A	N/A (ID_6)	
80	UID1-6	N/A	N/A (ID_7)	
81	UID1-11	N/A	N/A (ID_0)	
82	UID1-12	N/A	N/A (ID_1)	
83	UID1-13	N/A	N/A (ID_2)	
84	UID1-14	N/A	N/A (ID_3)	

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

6.4 Measurement of the GARC Bias Resistors and Voltages

This test may be omitted at the discretion of the Test Conductor.

Record the biasing resistors associated with the GARC in the table below. If assembly information (or visual inspection) is not available, power off the ACD electronics and make the following measurements on the circuit card (do not perform the measurement step on a conformally coated board). Indicate in the table if the biasing resistor values are either measured or taken from other documentation.

FREE Resistor	Value	Measured	Recorded from FREE Assembly Documentation
RG1			
RG2			
RG3			
RG4			
RG5			
RG6			
RG7			
RG8			
RG9			
RG10			

Using the DC multimeter, power on the FREE card and measure the following GARC bias voltages.

GARC Bias Signal	GARC Pin	Resistor Test Point	Expected Voltage (+/- 0.1 V)	Measured Voltage
HLD_WOR_BIAS	104	RG8	1.64	
BIAS_RCVR	156	RG6	1.10	
BIAS_DRV_H	160	RG3	1.53	
BIAS_DRV_L	169	RG1	1.75	
LVDS_PRESET_ADJ	184	RG9	1.52	

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

6.5 Measurement of the Power On Reset pulse

This section of the test will verify the width of the “PWR_ON_RST” pulse.

Turn off the power and connect a probe to TPR1. Setup the scope to capture a positive edge pulse 100 to 200mSec in width. Turn on the power and capture the pulse. Make a copy of the waveform and attach to the Test Record.

6.6 Measurement of the Power Supply Quality at the ACD Interface

This section of the test will verify the general functionality and performance of the power provided to the ACD at the interface while loaded with the nominal load of the ACD electronics assembly.

The ICD requires that the +3.3V supply be in the range of +3.20 to +3.60V referenced to the +3.3V return at the interface. Additionally, the RMS noise on this supply shall be less than 5 mV over a bandwidth of 1MHz and below. The FREE board will be tested from +3.00V to +3.60V at the interface.

The +28V supply to the high voltage bias supplies must be in the range of +27.0V to +29.0V referenced to the 28V return. The RMS noise on this supply shall be less than 10 mV over a bandwidth of 1 MHz and below.

Using a calibrated multimeter, measure the DC and RMS voltages at the following points and verify that they are within specification prior to proceeding. LAT commands to turn on power to the Primary and Secondary sides, respectively, will be required for these measurements. In situations where only one power supply is present, the Test Conductor shall make a note to this effect and skip the measurements which are not applicable.

This test may be omitted at the discretion of the Test Conductor.

Meas. No.	Signal Name	FREE Circuit Card Break Out Box V+ Probe	FREE Circuit Card Break Out Box RTN Probe	Measured DC Voltage	Expected DC Voltage	Measured RMS Voltage	Expected RMS Voltage
1	+3.3 V Primary	JP1-1	JP1-30		3.20 – 3.60		< 5 mV RMS
2	+28 V Primary	JP1-5	JP1-33		27.0 – 29.0		< 10 mV RMS
3	+3.3V Secondary	JS2-1	JS2-30		3.20 – 3.60		< 5 mV RMS
4	+28 V Secondary	JS2-5	JS2-33		27.0 – 29.0		< 10 mV RMS

Turn off the power supplies. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

7.0 Basic Aliveness Test

This section of the test will verify the general aliveness of the powered-on FREE circuit assembly. The initial power levels, the command and data interface, the DAC commanding, the GAFE test charge injection, and the pulse height analysis (PHA) circuitry will be checked for basic functionality. The pin connections for the two 79 pin circular connectors JP1 and JS2 are listed in Appendix 1. The pin connections for the two 9 pin MDM connectors to the High Voltage Bias Supplies are listed in Appendix 2.

7.1 GARC and GAFE Registers Initial Reset Test

This section will verify that GARC registers have been properly initialized during a reset command. The following test sequence of commands will perform this verification. This test will also verify that the GARC to AEM command and data return link is functional. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

Turn on the power supplies then -

1. Verify the external GARC Power On Reset pulse. If using the LabView GSE, send the Look at me and the Read All Values command.
2. Send the Veto_Delay_Rd command. The data field in the return data stream should be 5.
3. Send the HVBS_Level_Rd command. The data field in the return data stream should be 0.
4. Send the SAA_Level_Rd command. The data field in the return data stream should be 0.
5. Send the Hold_Delay_Rd command. The data field in the return data stream should be 28.
6. Send the Veto_Width_Rd command. The data field in the return data stream should be 2.
7. Send the HitMap_Width_Rd command. The data field in the return data stream should be 7.
8. Send the HitMap_Deadtime_Rd command. The data field in the return data stream should be 3.
9. Send the HitMap_Delay_Rd command. The data field in the return data stream should be 16.
10. Send the PHA_En0_Rd command. The data field in the return data stream should be 65535.
11. Send the PHA_En1_Rd command. The data field in the return data stream should be 3.
12. Send the Veto_En0_Rd command. The data field in the return data stream should be 65535.
13. Send the Veto_En1_Rd command. The data field in the return data stream should be 3.
14. Send the Max_PHA_Rd command. The data field in the return data stream should be 4.
15. Send the GARC_Mode_Rd command. The data field in the return data stream should be 768.
16. Send the GARC_Status command. The data field in the return data stream should be 24.
17. Send the GARC_Cmd_Reg command. The data field in the return data stream should be 0.
18. Send the GARC_Cmd_Rejects command. The data field in the return data stream should be 0.
19. Send the GARC_Version command. The data field in the return data stream should be 3 for GARC V3 ASICs.
20. Send the PHA_Thresh00_Rd command. The data field in the return data stream should be 1114.
21. Send the PHA_Thresh01_Rd command. The data field in the return data stream should be 1114.
22. Send the PHA_Thresh02_Rd command. The data field in the return data stream should be 1114.

23. Send the PHA_Thresh03_Rd command. The data field in the return data stream should be 1114.
24. Send the PHA_Thresh04_Rd command. The data field in the return data stream should be 1114.
25. Send the PHA_Thresh05_Rd command. The data field in the return data stream should be 1114.
26. Send the PHA_Thresh06_Rd command. The data field in the return data stream should be 1114.
27. Send the PHA_Thresh07_Rd command. The data field in the return data stream should be 1114.
28. Send the PHA_Thresh08_Rd command. The data field in the return data stream should be 1114.
29. Send the PHA_Thresh09_Rd command. The data field in the return data stream should be 1114.
30. Send the PHA_Thresh10_Rd command. The data field in the return data stream should be 1114.
31. Send the PHA_Thresh11_Rd command. The data field in the return data stream should be 1114.
32. Send the PHA_Thresh12_Rd command. The data field in the return data stream should be 1114.
33. Send the PHA_Thresh13_Rd command. The data field in the return data stream should be 1114.
34. Send the PHA_Thresh14_Rd command. The data field in the return data stream should be 1114.
35. Send the PHA_Thresh15_Rd command. The data field in the return data stream should be 1114.
36. Send the PHA_Thresh16_Rd command. The data field in the return data stream should be 1114.
37. Send the PHA_Thresh17_Rd command. The data field in the return data stream should be 1114.
38. Send the ADC_TACQ_Rd command. The data field in the return data stream should be 0.
39. Send the Trigger_ZS command (this captures the FREE board ID). FREE board ID should be as recorded on the WOA.

Record FREE board ID - _____

40. Send the GARC_Reset command (Do Reset Pulse from the Labview Program).
41. Check the FREE board ID it should be 255 indicating that a reset had occurred..
42. Verify the status of the GARC registers as shown in steps 2 – 39 above.

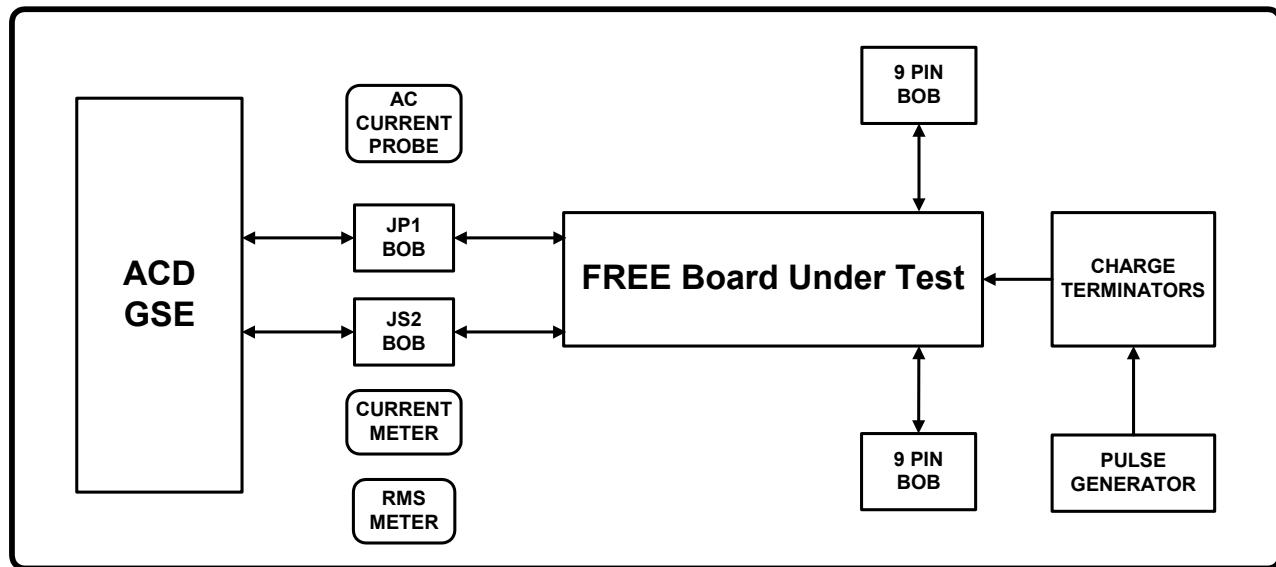
If all steps above have verified correctly, the GARC reset function has been verified. A summary of the initial reset parameters for GARC and GAFE is detailed below.

Register	Initial Value (decimal)	Initial Value (hex)
Veto_Delay	5	5
HVBS_Level	0	0
SAA_Level	0	0
Hold_Delay	28	1C
Veto_Width	2	2
HitMap_Width	7	7
HitMap_Deadtime	3	3
HitMap_Delay	16	10
PHA_EN0	65535	FFFF
PHA_EN1	3	3
VETO_EN0	65535	FFFF
VETO_EN1	3	3
Max_PHA	4	4
GARC_Mode	768	300
GARC_Status	24	18
Command_Register	0	0

GARC Diagnostic	0	0
Cmd Reject Ctr	0	0
FREE Board ID	*	*
GARC Version	1	1
PHA Threshold_00	1114	45A
PHA Threshold_01	1114	45A
PHA Threshold_02	1114	45A
PHA Threshold_03	1114	45A
PHA Threshold_04	1114	45A
PHA Threshold_05	1114	45A
PHA Threshold_06	1114	45A
PHA Threshold_07	1114	45A
PHA Threshold_08	1114	45A
PHA Threshold_09	1114	45A
PHA Threshold_10	1114	45A
PHA Threshold_11	1114	45A
PHA Threshold_12	1114	45A
PHA Threshold_13	1114	45A
PHA Threshold_14	1114	45A
PHA Threshold_15	1114	45A
PHA Threshold_16	1114	45A
PHA Threshold_17	1114	45A
ADC TACQ	0	0
GAFE Mode	48	30
GAFE VETO DAC	57	39
GAFE VETO VERNIER	38	26
GAFE HLD DAC	55	37
GAFE BIAS DAC	32	20
GAFE TCI DAC	0	0
GAFE Wr Ctr	0	0
GAFE Reject Ctr	0	0

8.0 Testing the FREE Electronics via Command-Response Protocol

The GARC logic is based on a command-response protocol and requires an AEM or AEM simulator to access the logic functions. For each of the following commands, the proper GARC and/or GAFE response may be tested. Note that all GAFEs will respond to a broadcast write command (e.g., GAFE address of decimal 31), but a read command requires a unique GAFE address. The following test details the proper sequence for a single GARC ASIC. The steps are numbered for easier reference. The test setup required is detailed in the diagram below.



8.1 FREE Power Measurement at the Nominal Power Supply Voltage

Verify that the GARC power supply is set to +3.30V. After initial power up, measure the +3.30V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.3V Current Measured (mA)	+3.3V Current Expected (mA)
LVDS "A" Drivers Enabled			
LVDS "B" Drivers Enabled	768		200 ± 10mA

LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		$150 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		$150 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		$95 \pm 10\text{mA}$

8.2 FREE Power Measurement at the Minimum Power Supply Voltage

Verify that the GARC power supply is set to +3.0V. After initial power up, measure the +3.0V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.0V Current Measured (mA)	+3.0V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		$170 \pm 10\text{mA}$
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		$125 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		$125 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		$75 \pm 10\text{mA}$

8.3 FREE Power Measurement at the Maximum Power Supply Voltage

Verify that the GARC power supply is set to +3.6V. After initial power up, measure the +3.6V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.6V Current Measured (mA)	+3.6V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		$230 \pm 10\text{mA}$
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		$175 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		$175 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		$115 \pm 10\text{mA}$

5. Reset the GARC power supply to +3.3V.
6. Send the GARC_Reset command to return the GARC to the initial power-on configuration.

8.4 GARC/GAFE Register Read/Write Tests

This section tests the proper functioning of each bit of the commandable registers in the GARC. The intent is to toggle each bit in a variety of patterns to ensure that all bits are addressable and that there is no stuck-at-fault condition. This can be accomplished using the LabView GSE software by doing the Register Test 3 times with all GAFE registers enabled.

After running the script proceed to step 8.44.

The following GARC registers will be tested in this section:

GARC Register Name	Register Width (bits)	Register Type
Veto_Delay	5	Read/Write
HVBS_Level	12	Read/Write
SAA_Level	12	Read/Write
Hold_Delay	7	Read/Write
Veto_Width	3	Read/Write
HitMap_Width	4	Read/Write
HitMap_Deadtime	3	Read/Write
HitMap_Delay	5	Read/Write
PHA_En0	16	Read/Write
PHA_En1	2	Read/Write
VETO_En0	16	Read/Write
VETO_En1	2	Read/Write
Max_PHA	5	Read/Write
GARC_Mode	11	Read/Write
GARC_Status	6	Read Only
Command_Register	16	Read Only
GARC_Diagnostic	16	Read Only
Cmd_Reject_Counter	8	Read Only

FREE Board ID	8	Read Only
GARC Version	3	Read Only
PHA Threshold_00	16	Read/Write
PHA Threshold_01	16	Read/Write
PHA Threshold_02	16	Read/Write
PHA Threshold_03	16	Read/Write
PHA Threshold_04	16	Read/Write
PHA Threshold_05	16	Read/Write
PHA Threshold_06	16	Read/Write
PHA Threshold_07	16	Read/Write
PHA Threshold_08	16	Read/Write
PHA Threshold_09	16	Read/Write
PHA Threshold_10	16	Read/Write
PHA Threshold_11	16	Read/Write
PHA Threshold_12	16	Read/Write
PHA Threshold_13	16	Read/Write
PHA Threshold_14	16	Read/Write
PHA Threshold_15	16	Read/Write
PHA Threshold_16	16	Read/Write
PHA Threshold_17	16	Read/Write
ADC_TACQ	6	Read/Write

8.5 Veto Delay Register Test

1. Send the Veto_Delay_Wr command with a data argument of 5'h0 (0). Send the Veto_Delay_Rd command and read back this commanded data argument.
2. Send the Veto_Delay_Wr command with a data argument of 5'h15 (21). Send the Veto_Delay_Rd command and read back this commanded data argument.
3. Send the Veto_Delay_Wr command with a data argument of 5'h0A (10). Send the Veto_Delay_Rd command and read back this commanded data argument.
4. Send the Veto_Delay_Wr command with a data argument of 5'h1F (31). Send the Veto_Delay_Rd command and read back this commanded data argument.
5. Send the Veto_Delay_Wr command with a data argument of 5'h5 (5). Send the Veto_Delay_Rd command and read back this commanded data argument.

8.6 HVBS Level Register Test

1. Send the HVBS_Level_Wr command with a data argument of 12'h0 (0). Send the HVBS_Level_Rd command and read back this commanded data argument.
2. Send the HVBS_Level_Wr command with a data argument of 12'h555 (1365). Send the HVBS_Level_Rd command and read back this commanded data argument.
3. Send the HVBS_Level_Wr command with a data argument of 12'hAAA (2730). Send the HVBS_Level_Rd command and read back this commanded data argument.
4. Send the HVBS_Level_Wr command with a data argument of 12'hFFF (4095). Send the HVBS_Level_Rd command and read back this commanded data argument.
5. Send the HVBS_Level_Wr command with a data argument of 12'h0 (0). Send the HVBS_Level_Rd command and read back this commanded data argument.

8.7 SAA Level Register Test

1. Send the SAA_Level_Wr command with a data argument of 12'h0 (0). Send the SAA_Level_Rd command and read back this commanded data argument.
2. Send the SAA_Level_Wr command with a data argument of 12'h555 (1365). Send the SAA_Level_Rd command and read back this commanded data argument.
3. Send the SAA_Level_Wr command with a data argument of 12'hAAA (2730). Send the SAA_Level_Rd command and read back this commanded data argument.
4. Send the SAA_Level_Wr command with a data argument of 12'hFFF (4095). Send the SAA_Level_Rd command and read back this commanded data argument.
5. Send the SAA_Level_Wr command with a data argument of 12'h0 (0). Send the SAA_Level_Rd command and read back this commanded data argument.

8.8 Hold Delay Register Test

1. Send the Hold_Delay_Wr command with a data argument of 7'h0 (0). Send the Hold_Delay_Rd command and read back this commanded data argument.
2. Send the Hold_Delay_Wr command with a data argument of 7'h55 (85). Send the Hold_Delay_Rd command and read back this commanded data argument.
3. Send the Hold_Delay_Wr command with a data argument of 7'h2A (42). Send the Hold_Delay_Rd command and read back this commanded data argument.
4. Send the Hold_Delay_Wr command with a data argument of 7'h7F (127). Send the Hold_Delay_Rd command and read back this commanded data argument.
5. Send the Hold_Delay_Wr command with a data argument of 7'h1C (28). Send the Hold_Delay_Rd command and read back this commanded data argument.

8.9 Veto Width Register Test

1. Send the Veto_Width_Wr command with a data argument of 3'h0 (0). Send the Veto_Width_Rd command and read back this commanded data argument.
2. Send the Veto_Width_Wr command with a data argument of 3'h5 (5). Send the Veto_Width_Rd command and read back this commanded data argument.
3. Send the Veto_Width_Wr command with a data argument of 3'h7 (7). Send the Veto_Width_Rd command and read back this commanded data argument.
4. Send the Veto_Width_Wr command with a data argument of 3'h2 (2). Send the Veto_Width_Rd command and read back this commanded data argument.

8.10 HitMap Width Register Test

1. Send the HitMap_Width_Wr command with a data argument of 4'h0 (0). Send the HitMap_Width_Rd command and read back this commanded data argument.
2. Send the HitMap_Width_Wr command with a data argument of 4'h5 (5). Send the HitMap_Width_Rd command and read back this commanded data argument.
3. Send the HitMap_Width_Wr command with a data argument of 4'hA (10). Send the HitMap_Width_Rd command and read back this commanded data argument.

4. Send the HitMap_Width_Wr command with a data argument of 4'hF (15). Send the HitMap_Width_Rd command and read back this commanded data argument.
5. Send the HitMap_Width_Wr command with a data argument of 4'h7 (7). Send the HitMap_Width_Rd command and read back this commanded data argument.

8.11 HitMap Deadtime Register Test

1. Send the HitMap_Deadtime_Wr command with a data argument of 3'h0 (0). Send the HitMap_Deadtime_Rd command and read back this commanded data argument.
2. Send the HitMap_Deadtime_Wr command with a data argument of 3'h5 (5). Send the HitMap_Deadtime_Rd command and read back this commanded data argument.
3. Send the HitMap_Deadtime_Wr command with a data argument of 3'h2 (2). Send the HitMap_Deadtime_Rd command and read back this commanded data argument.
4. Send the HitMap_Deadtime_Wr command with a data argument of 3'h7 (7). Send the HitMap_Deadtime_Rd command and read back this commanded data argument.
5. Send the HitMap_Deadtime_Wr command with a data argument of 3'h3 (3). Send the HitMap_Deadtime_Rd command and read back this commanded data argument.

8.12 HitMap Delay Register Test

1. Send the HitMap_Delay_Wr command with a data argument of 5'h0 (0). Send the HitMap_Delay_Rd command and read back this commanded data argument.
2. Send the HitMap_Delay_Wr command with a data argument of 5'h15 (21). Send the HitMap_Delay_Rd command and read back this commanded data argument.
3. Send the HitMap_Delay_Wr command with a data argument of 5'h0A (10). Send the HitMap_Delay_Rd command and read back this commanded data argument.
4. Send the HitMap_Delay_Wr command with a data argument of 5'h1F (31). Send the HitMap_Delay_Rd command and read back this commanded data argument.
5. Send the HitMap_Delay_Wr command with a data argument of 5'h10 (16). Send the HitMap_Delay_Rd command and read back this commanded data argument.

8.13 PHA En0 Register Test

1. Send the PHA_En0_Wr command with a data argument of 16'h0 (0). Send the PHA_En0_Rd command and read back this commanded data argument.
2. Send the PHA_En0_Wr command with a data argument of 16'h5555 (21845). Send the PHA_En0_Rd command and read back this commanded data argument.
3. Send the PHA_En0_Wr command with a data argument of 16'hAAAA (43690). Send the PHA_En0_Rd command and read back this commanded data argument.
4. Send the PHA_En0_Wr command with a data argument of 16'hFFFF (65535). Send the PHA_En0_Rd command and read back this commanded data argument.

8.14 Veto En0 Register Test

1. Send the VETO_En0_Wr command with a data argument of 16'h0 (0). Send the VETO_En0_Rd command and read back this commanded data argument.
2. Send the VETO_En0_Wr command with a data argument of 16'h5555 (21845). Send the VETO_En0_Rd command and read back this commanded data argument.
3. Send the VETO_En0_Wr command with a data argument of 16'hAAAA (43690). Send the VETO_En0_Rd command and read back this commanded data argument.
4. Send the VETO_En0_Wr command with a data argument of 16'hFFFF (65535). Send the VETO_En0_Rd command and read back this commanded data argument.

8.15 PHA En1 Register Test

1. Send the PHA_En1_Wr command with a data argument of 2'h0 (0). Send the PHA_En1_Rd command and read back this commanded data argument.
2. Send the PHA_En1_Wr command with a data argument of 2'h1 (1). Send the PHA_En1_Rd command and read back this commanded data argument.
3. Send the PHA_En1_Wr command with a data argument of 2'h2 (2). Send the PHA_En1_Rd command and read back this commanded data argument.
4. Send the PHA_En1_Wr command with a data argument of 2'h3 (3). Send the PHA_En1_Rd command and read back this commanded data argument.

8.16 Veto En1 Register Test

1. Send the VETO_En1_Wr command with a data argument of 2'h0 (0). Send the VETO_En1_Rd command and read back this commanded data argument.
2. Send the VETO_En1_Wr command with a data argument of 2'h1 (1). Send the VETO_En1_Rd command and read back this commanded data argument.
3. Send the VETO_En1_Wr command with a data argument of 2'h2 (2). Send the VETO_En1_Rd command and read back this commanded data argument.
4. Send the VETO_En1_Wr command with a data argument of 2'h3 (3). Send the VETO_En1_Rd command and read back this commanded data argument.

8.17 MaxPHA Register Test

1. Send the MaxPHA_Wr command with a data argument of 5'h0 (0). Send the MaxPHA_Rd command and read back this commanded data argument.
2. Send the MaxPHA_Wr command with a data argument of 5'h15 (21). Send the MaxPHA_Rd command and read back this commanded data argument.
3. Send the MaxPHA_Wr command with a data argument of 5'h0A (10). Send the MaxPHA_Rd command and read back this commanded data argument.
4. Send the MaxPHA_Wr command with a data argument of 5'h1F (31). Send the MaxPHA_Rd command and read back this commanded data argument.
5. Send the MaxPHA_Wr command with a data argument of 5'h4 (4). Send the MaxPHA_Rd command and read back this commanded data argument.

8.18 GARC Mode Register Test

1. Send the GARC_Mode_Wr command with a data argument of 11'h2 (2). Send the GARC_Mode_Rd command and read back this commanded data argument.
2. Send the GARC_Mode_Wr command with a data argument of 11'h4 (4). Send the GARC_Mode_Rd command and read back this commanded data argument.
3. Send the GARC_Mode_Wr command with a data argument of 11'h8 (8). Send the GARC_Mode_Rd command and read back this commanded data argument.
4. Send the GARC_Mode_Wr command with a data argument of 11'h10 (16). Send the GARC_Mode_Rd command and read back this commanded data argument.
5. Send the GARC_Mode_Wr command with a data argument of 11'h20 (32). Send the GARC_Mode_Rd command and read back this commanded data argument.
6. Send the GARC_Mode_Wr command with a data argument of 11'h40 (64). Send the GARC_Mode_Rd command and read back this commanded data argument.
7. Send the GARC_Mode_Wr command with a data argument of 11'h80 (128). Send the GARC_Mode_Rd command and read back this commanded data argument.
8. Send the GARC_Mode_Wr command with a data argument of 11'h100 (256). Send the GARC_Mode_Rd command and read back this commanded data argument.
9. Send the GARC_Mode_Wr command with a data argument of 11'h200 (512). Send the GARC_Mode_Rd command and read back this commanded data argument.
10. Send the GARC_Mode_Wr command with a data argument of 11'h400 (1024). Send the GARC_Mode_Rd command and read back this commanded data argument.
11. Send the GARC_Mode_Wr command with a data argument of 11'h300 (768). Send the GARC_Mode_Rd command and read back this commanded data argument.

8.19 PHA Threshold Channel 00 Register Test

1. Send the PHA_Thresh00_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh00_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh00_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh00_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh00_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh00_Rd command and read back this commanded data argument.

8.20 PHA Threshold Channel 01 Register Test

1. Send the PHA_Thresh01_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh01_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh01_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh01_Rd command and read back this commanded data argument.

3. Send the PHA_Thresh01_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh01_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh01_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh01_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh01_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh01_Rd command and read back this commanded data argument.

8.21 PHA Threshold Channel 02 Register Test

1. Send the PHA_Thresh02_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh02_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh02_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh02_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh02_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh02_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh02_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh02_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh02_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh02_Rd command and read back this commanded data argument.

8.22 PHA Threshold Channel 03 Register Test

1. Send the PHA_Thresh03_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh03_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh03_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh03_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh03_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh03_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh03_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh03_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh03_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh03_Rd command and read back this commanded data argument.

8.23 PHA Threshold Channel 04 Register Test

1. Send the PHA_Thresh04_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh04_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh04_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh04_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh04_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh04_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh04_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh04_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh04_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh04_Rd command and read back this commanded data argument.

8.24 PHA Threshold Channel 05 Register Test

1. Send the PHA_Thresh05_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh05_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh05_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh05_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh05_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh05_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh05_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh05_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh05_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh05_Rd command and read back this commanded data argument.

8.25 PHA Threshold Channel 06 Register Test

1. Send the PHA_Thresh06_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh06_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh06_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh06_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh06_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh06_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh06_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh06_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh06_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh06_Rd command and read back this commanded data argument.

8.26 PHA Threshold Channel 07 Register Test

1. Send the PHA_Thresh07_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh07_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh07_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh07_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh07_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh07_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh07_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh07_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh07_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh07_Rd command and read back this commanded data argument.

8.27 PHA Threshold Channel 08 Register Test

1. Send the PHA_Thresh00_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh00_Rd command and read back this commanded data argument.

2. Send the PHA_Thresh00_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh00_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh00_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh00_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh00_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh00_Rd command and read back this commanded data argument.

8.28 PHA Threshold Channel 09 Register Test

1. Send the PHA_Thresh09_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh09_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh09_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh09_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh09_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh09_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh09_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh09_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh09_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh09_Rd command and read back this commanded data argument.

8.29 PHA Threshold Channel 10 Register Test

1. Send the PHA_Thresh10_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh10_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh10_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh10_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh10_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh10_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh10_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh10_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh10_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh10_Rd command and read back this commanded data argument.

8.30 PHA Threshold Channel 11 Register Test

1. Send the PHA_Thresh11_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh11_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh11_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh11_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh11_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh11_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh11_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh11_Rd command and read back this commanded data argument.

5. Send the PHA_Thresh11_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh11_Rd command and read back this commanded data argument.

8.31 PHA Threshold Channel 12 Register Test

1. Send the PHA_Thresh12_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh12_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh12_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh12_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh12_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh12_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh12_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh12_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh12_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh12_Rd command and read back this commanded data argument.

8.32 PHA Threshold Channel 13 Register Test

1. Send the PHA_Thresh13_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh13_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh13_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh13_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh13_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh13_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh13_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh13_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh13_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh13_Rd command and read back this commanded data argument.

8.33 PHA Threshold Channel 14 Register Test

1. Send the PHA_Thresh14_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh14_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh14_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh14_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh14_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh14_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh14_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh14_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh14_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh14_Rd command and read back this commanded data argument.

8.34 PHA Threshold Channel 15 Register Test

1. Send the PHA_Thresh15_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh15_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh15_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh15_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh15_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh15_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh15_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh15_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh15_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh15_Rd command and read back this commanded data argument.

8.35 PHA Threshold Channel 16 Register Test

1. Send the PHA_Thresh16_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh16_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh16_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh16_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh16_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh16_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh16_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh16_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh16_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh16_Rd command and read back this commanded data argument.

8.36 PHA Threshold Channel 17 Register Test

1. Send the PHA_Thresh17_Wr command with a data argument of 12'h0 (0). Send the PHA_Thresh17_Rd command and read back this commanded data argument.
2. Send the PHA_Thresh17_Wr command with a data argument of 12'h555 (1365). Send the PHA_Thresh17_Rd command and read back this commanded data argument.
3. Send the PHA_Thresh17_Wr command with a data argument of 12'hAAA (2730). Send the PHA_Thresh17_Rd command and read back this commanded data argument.
4. Send the PHA_Thresh17_Wr command with a data argument of 12'hFFF (4095). Send the PHA_Thresh17_Rd command and read back this commanded data argument.
5. Send the PHA_Thresh17_Wr command with a data argument of 12'h45A (1114). Send the PHA_Thresh17_Rd command and read back this commanded data argument.

8.37 ADC TACQ Register Test

1. Send the ADC_TACQ_Wr command with a data argument of 6'h0 (0). Send the ADC_TACQ_Rd command and read back this commanded data argument.
2. Send the ADC_TACQ_Wr command with a data argument of 6'h15 (21). Send the ADC_TACQ_Rd command and read back this commanded data argument.

3. Send the ADC_TACQ_Wr command with a data argument of 6'h2A (42). Send the ADC_TACQ_Rd command and read back this commanded data argument.
4. Send the ADC_TACQ_Wr command with a data argument of 6'h3F (63). Send the ADC_TACQ_Rd command and read back this commanded data argument.
5. Send the ADC_TACQ_Wr command with a data argument of 6'h0 (0). Send the ADC_TACQ_Rd command and read back this commanded data argument.
6. Send the GARC_Reset command to ensure all registers are at the proper initial value.

At the successful conclusion of this section, the GARC commandable register bits have been demonstrated to be functional with all bits toggling as commanded.

Now the GAFE Registers for each ASIC Connected to the GARC can be tested.

8.38 GAFE ASICs Mode Register Test

This section tests the proper functioning of the GAFE mode register. Repeat for all GAFE ASICs present using valid GAFE addressing.

1. Send the GAFE_Config_Write command to the GAFE being tested with a data field of 16'h00 (0).
2. Send the GAFE_Config_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_Config_Write command to the GAFE being tested with a data field of 16'hFF (255).
4. Send the GAFE_Config_Read command. The data field in the return data stream should be 16'hFF (255).
5. Send the GAFE_Config_Write command to the GAFE being tested with a data field of 16'h30 (48).
6. Send the GAFE_Config_Read command. The data field in the return data stream should be 16'h30 (48).

8.39 GAFE ASIC VETO DAC Register Test

This section tests the proper functioning of the GAFE VETO DAC register. Repeat for all GAFE ASICs present, using valid GAFE addressing.

1. Send the GAFE_VETO_Write command to the GAFE being tested with a data field of 16'h00 (0).
2. Send the GAFE_VETO_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_VETO_Write command to the GAFE being tested with a data field of 16'h3F (63).
4. Send the GAFE_VETO_Read command. The data field in the return data stream should be 16'h3F (63).
5. Send the GAFE_VETO_Write command to the GAFE being tested with a data field of 16'h39 (57).
6. Send the GAFE_VETO_Read command. The data field in the return data stream should be 16'h39 (57).

8.40 GAFE ASIC VETO VERNIER Register Test

This section tests the proper functioning of the GAFE VETO VERNIER register. Repeat for all GAFE ASICs present, using valid GAFE addressing.

1. Send the GAFE_VERNIER_Write command to the GAFE being tested with a data field of 16'h00 (0).
2. Send the GAFE_VERNIER_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_VERNIER_Write command to the GAFE being tested with a data field of 16'h3F (63).
4. Send the GAFE_VERNIER_Read command. The data field in the return data stream should be 16'h3F (63).
5. Send the GAFE_VERNIER_Write command to the GAFE being tested with a data field of 16'h26 (38).
6. Send the GAFE_VERNIER_Read command. The data field in the return data stream should be 16'h26 (38).

8.41 GAFE ASIC HLD DAC Register Test

This section tests the proper functioning of the GAFE HLD_DAC register. Repeat for all GAFE ASICS present, using valid GAFE addressing.

1. Send the GAFE_HLD_Write command to the GAFE being tested with a data field of 16'h00 (0).
2. Send the GAFE_HLD_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_HLD_Write command to the GAFE being tested with a data field of 16'h3F (63).
4. Send the GAFE_HLD_Read command. The data field in the return data stream should be 16'h3F (63).
5. Send the GAFE_HLD_Write command to the GAFE being tested with a data field of 16'h37 (55).
6. Send the GAFE_HLD_Read command. The data field in the return data stream should be 16'h37 (55).

8.42 GAFE ASIC BIAS DAC Register Test

This section tests the proper functioning of the GAFE BIAS_DAC register. Repeat for all GAFE ASICS present, using valid GAFE addressing.

1. Send the GAFE_BIAS_Write command to the GAFE being tested with a data field of 16'h00 (0).
2. Send the GAFE_BIAS_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_BIAS_Write command to the GAFE being tested with a data field of 16'h3F (63).
4. Send the GAFE_BIAS_Read command. The data field in the return data stream should be 16'h3F (63).
5. Send the GAFE_BIAS_Write command to the GAFE being tested with a data field of 16'h20 (32).
6. Send the GAFE_BIAS_Read command. The data field in the return data stream should be 16'h20 (32).

8.43 GAFE ASIC TCI DAC Register Test

This section tests the proper functioning of the GAFE TCI_DAC register. Repeat for all GAFE ASICS present, using valid GAFE addressing.

1. Send the GAFE_TCI_Write command to the GAFE being tested with a data field of 16'h00 (0).

2. Send the GAFE_TCI_Read command. The data field in the return data stream should be 16'h00 (0).
3. Send the GAFE_TCI_Write command to the GAFE being tested with a data field of 16'h3F (63).
4. Send the GAFE_TCI_Read command. The data field in the return data stream should be 16'h3F (63).
5. Send the GAFE_TCI_Write command to the GAFE being tested with a data field of 16'h00 (0).
6. Send the GAFE_TCI_Read command. The data field in the return data stream should be 16'h00 (0).

At the successful conclusion of this register test section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

Testing the GAFE Logic for each ASIC Connected to the GARC

At this point in the FREE functional test, functional testing of the logic for any GAFEs connected to the GARC may be performed. Nominally, the flight FREE cards will have 18 GAFEs on the board, but some engineering-model FREE cards may have fewer. A minimum of one GAFE ASIC (or the GAFE logic simulator) must be connected for this test. If multiple GAFE logic cores are to be tested concurrently, such as the nominal condition for a populated FREE circuit card, then each address may be tested in sequence, replicating the steps detailed in the GAFE logic test procedure. Each GAFE is independent and the commands for each test may be performed either in series or in parallel up to a total of 18 GAFE ASICs.

8.44 Initial GAFE Logic Reset Test

After initial power up or a GARC Reset command is sent, the GAFE registers should be initialized. This is tested by the following command sequence (sent to each GAFE being tested at the unique five bit address for that GAFE). This test may be automated using the LabView GSE via the **GAFE LOGIC RESET TEST.TXT** script.

1. Send the GARC_Reset command.
2. Send the GAFE_Config_Read command. The data field in the return data stream should be 16'h30 (48).
3. Send the GAFE_Version Command. The GAFE Version indicates the version of the GAFE logic core and should be 3.
4. Send the GAFE_VETO_Read command. The data field in the return data stream should be 16'h39 (57).
5. Send the GAFE_VERNIER_Read command. The data field in the return data stream should be 16'h26 (38).
6. Send the GAFE_HLD_Read command. The data field in the return data stream should be 16'h37 (55).
7. Send the GAFE_BIAS_Read command. The data field in the return data stream should be 16'h20 (32).
8. Send the GAFE_TCI_Read command. The data field in the return data stream should be 16'h00 (0).
9. Send the GAFE_Version command. The data field in the return data stream should be 16'h03 (3).
10. Send the GAFE_Write_Ctr command. The data field in the return data stream should be 16'h00 (0).
11. Send the GAFE_Reject_Ctr command. The data field in the return data stream should be 16'h00 (0).

12. Send the GAFE_Cmd_Ctr command. The data field in the return data stream should be 16'h0A (10).
13. Send the GAFE_Chip_Address command for each of the 18 GAFE's. The data field in the return data stream should be the address of the chip that was commanded.
14. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.45 GAFE ASIC Broadcast Command Functional Verification

This section tests the proper response to broadcast commands (e.g., address 31) by the GAFEs.

This test may be automated using the LabView GSE via the **GAFE Broadcast Command Test.txt** script.

1. Send the GARC_Reset command.
2. Send the GAFE_Config_Read command with a broadcast address, i.e., address 'h1F (31), to all the GAFEs being tested. There should be no data returned from any GAFE.
3. Send the GAFE_Config_Write command with a broadcast address and a data field of 'hAA (170) to the GAFEs.
4. Send a GAFE_Config_Read address command to each GAFE under test. The return data field from each addressed GAFE should be 'hAA (170).
5. Send a GARC_Reset command to reinitialize each of the GAFE logic cores.
6. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.46 Test of the GARC Parity Error Detection and Error Generation

This section tests the proper functioning of the GARC return data parity select bit and the GARC's ability to detect command and data parity errors.

This test may be automated using the LabView GSE via the **GARC Parity Test.txt** script.

1. Send the GARC_Reset command.
2. Send the GARC_Status command. The data field in the return data stream should be decimal 24.
3. Send the GARC_Mode command with a data argument of decimal 769, a command to return event data with even parity.
4. Send the GARC_Status command. The data field in the return data stream should show an AEM parity error.
5. Send the GARC_Mode command with a data argument of decimal 768, a command back to odd parity, the nominal mode.
6. Send the GARC_Status command. The data field in the return data stream should be decimal 24. The AEM should indicate nominal parity (no errors).
7. Send the GARC_Reset command to reinitialize all GARC registers. Ready to test Command and Data parity errors.
8. Send the GARC_Diagnostic command and verify that bits 15:12 in the return data word are 4'b0000.

9. Send the GARC_Version command.
10. Send the GARC_Diagnostic command and verify that bits 15:12 in the return data word are 4'b0000.
11. Send the Command_Register command and verify that the return data is 16'h0000.
12. Send the even command parity (i.e., error) command: 34'h2404C0001.
13. Send the GARC_Diagnostic command and verify that bits 15:12 in the return data word are 4'b1101.
14. Send the Command_Register command and verify that the return data is 16'h404E.
15. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.47 Test of the Look-At-Me Circuitry

This section tests the proper functioning of the GARC Look-At-Me circuitry. The GARC has the capability to receive commands from either the primary side or secondary side. The selection of which set of receivers to listen to is controlled by the Look-At-Me circuitry. This circuitry toggles the status of the receiving side based upon receipt of a special command pattern (e.g., **34'h24153D721**). This is the equivalent of sending a GARC configuration command to addr 1, function 4, with a data pattern of 60304.

Another way to look at the bit pattern (in a format like the ICD would present it) would be:

1001	==	configuration command
0	==	GARC
00001	==	address 1
0	==	write
1	==	a command with data
0100	==	function 4
1	==	command parity
16'h	==	EB90 == data field (60304)
0	==	data parity

This test may be automated using the LabView GSE via the [GARC Look At Me Test.txt](#) script.

Turn on the system and send a Look-at-me command. Send the GARC_Status command. The data field in the return data stream should be decimal 24. Bit 0 (LSB) of the Status register represents the Look-At-Me status (0 = A, 1 = B).. Set the GSE to the Secondary side, Send the GARC_Status command. Observe that there is no response from the GARC.

Send the Look_At_Me command to the GARC from the secondary side interface. Send the GARC_Status command. The data field in the return data should be decimal 25 (with the LSB = 1, indicating the Look-At-Me status is B side). Set the GSE for the Primary side and send the GARC_Status command. Observe that there is no response from the GARC. Send the Look_At_Me command to the GARC from the primary side interface. Send the GARC_Status command. The data field in the return data should be decimal 24 (with the LSB = 0, indicating the Look-At-Me status is A side).

This concludes the test of the GARC Look-At-Me circuitry. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.48 Maximum PHA Return Test

This section tests the proper functioning of the event data processor as it handles the Maximum Number of PHA words command.

This test may be automated using the LabView GSE via the [GARC Max PHA Return Test.tst](#) script.

1. Send the Max_PHA_Wr command with a data argument of 18. Send the Max_PHA_Rd command and verify that the data value has been set. Send the Trigger_ZS command and verify that the event data processor sends back 18 PHA words.
2. Repeat the previous step with a data argument of 17.
3. Repeat the previous step with a data argument of 16.
4. Repeat the previous step with a data argument of 15.
5. Repeat the previous step with a data argument of 14.
6. Repeat the previous step with a data argument of 13.
7. Repeat the previous step with a data argument of 12.
8. Repeat the previous step with a data argument of 11.
9. Repeat the previous step with a data argument of 10.
10. Repeat the previous step with a data argument of 9.
11. Repeat the previous step with a data argument of 8.
12. Repeat the previous step with a data argument of 7.
13. Repeat the previous step with a data argument of 6.
14. Repeat the previous step with a data argument of 5.
15. Repeat the previous step with a data argument of 4.
16. Repeat the previous step with a data argument of 3.
17. Repeat the previous step with a data argument of 2.
18. Repeat the previous step with a data argument of 1.
19. Repeat the previous step with a data argument of 0.
20. Send the GARC_Reset command to restore the Max_PHA number to the default. This completes the test of the GARC MAX_PHA function. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.49 PHA Enable/Disable Test

This section tests the proper functioning of the event data processor as it handles the PHA enables and disables in selection of PHA words for transmission.

This test may be automated using the LabView GSE via the [GARC PHA Enable Test.tst](#) script.

1. Send the PHA_En0_Wr command with a data argument of decimal ‘hFFFF (65535). Verify this value with the PHA_En0_Rd command. This enables channels 0 – 15.
2. Send the PHA_En1_Wr command with a data argument of decimal 3. Verify this value with the PHA_En1_Rd command. This enables channels 16 and 17.

3. Send the Trigger_NOZS command. The event data processor should respond with 18 PHA words during event readout.
4. Send the PHA_En0_Wr command with a data argument of ‘hFFFE (65534). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 0.
5. Send the PHA_En0_Wr command with a data argument of ‘hFFFD (65533). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 1.
6. Send the PHA_En0_Wr command with a data argument of ‘hFFFB (65531). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 2.
7. Send the PHA_En0_Wr command with a data argument of ‘hFFF7 (65527). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 3.
8. Send the PHA_En0_Wr command with a data argument of ‘hFFEF (65519). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 4.
9. Send the PHA_En0_Wr command with a data argument of ‘hFFDF (65503). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 5.
10. Send the PHA_En0_Wr command with a data argument of ‘hFFBF (65471). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 6.
11. Send the PHA_En0_Wr command with a data argument of ‘hFF7F (65407). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 7.
12. Send the PHA_En0_Wr command with a data argument of ‘hFEFF (65279). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 8.
13. Send the PHA_En0_Wr command with a data argument of ‘hFDFF (65023). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 9.
14. Send the PHA_En0_Wr command with a data argument of ‘hFBFF (64511). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 10.
15. Send the PHA_En0_Wr command with a data argument of ‘hF7FF (63487). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 11.
16. Send the PHA_En0_Wr command with a data argument of ‘hEFFF (61439). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 12.
17. Send the PHA_En0_Wr command with a data argument of ‘hDFFF (57343). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 13.

18. Send the PHA_En0_Wr command with a data argument of 'hBFFF (49151). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 14.
19. Send the PHA_En0_Wr command with a data argument of 'h7FFF (32767). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 15.
20. Send the PHA_En0_Wr command with a data argument of 'hFFFF (65535). Verify this value with the PHA_En0_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words.
21. Send the PHA_En1_Wr command with a data argument of 2. Verify this value with the PHA_En1_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 16.
22. Send the PHA_En1_Wr command with a data argument of 1. Verify this value with the PHA_En1_Rd command. Send the Trigger_NOZS command. The event processor should respond with all PHA words except channel 17.
23. Send the GARC_Reset command to reinitialize all GARC registers. This completes the testing of the PHA enable and disable register bits. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

8.50 PHA Threshold Verification Test

This section tests the proper functioning of each of the 18 PHA thresholding circuits. The intent of the circuits is such that the ZS Map bit is set active high for a given PHA word if either the range bit is high or the 12 bit PHA word is greater than the PHA threshold.

This test may be automated using the LabView GSE via the **GARC PHA Threshold Test.txt** script.

1. Send the GARC_Reset command.
2. Send the Max_PHA_Wr command with a data argument of 18.
3. Send the GAFE Config Wr command with a data argument of 50 (enable TCI) to channel 0.
4. Send the GAFE TCI Wr command with a data argument of 10 to channel 0.
5. Send the PHA_Thresh00 Wr command with a data argument of 100.
6. Repeat these steps for channels 01 through 17.
7. Send the TRIG_ZS command. All 18 channels of PHA should be returned.
8. Send the PHA_Thresh00_Wr command with a data argument of 3000. Verify with the PHA_Thresh00_Rd command.
9. Send the TRIG_ZS command. All PHA channels except for channel 0 should be returned in the event data.
10. Send the PHA_Thresh01_Wr command with a data argument of 3000 and set PHA_Thresh00 back to 100. Verify with the PHA_Thresh_Rd command.
11. Send the TRIG_ZS command. All PHA channels except for channel 1 should be returned in the event data.
12. Repeat the above two steps serially for channels 2 – 17, verifying in each case that the proper event word is zero suppressed in the event data.
13. Send the GARC_Reset command to restore all values to the power-on defaults.

This completes the PHA Threshold Verification section of the procedure. Record the successful completion of this test in the Test Record at the end of this procedure.

8.51 Data Phase Command

This section tests the ability of the Data Phase Command to change the Clock edge that shifts the out to the AEM.

This test may be omitted at the discretion of the Test Conductor.

1. Connect scope probes to the GSE board at J9-7 (Clock A) and to J8-6 (NSData A).
2. Send the GARC Reset command.
3. Send the GARC_Mode Read command. Should have a data argument of decimal 768. Monitor the scope to verify that the Data is shifted out on the positive edge of Clock. Capture scope traces with a picture and attach to the Test Record.4. Send the GARC_Mode_Wr command with a data argument of decimal 2816 to change the Data Phase.
5. Send the GARC_Mode Read command. Should have a data argument of decimal 2816. Monitor the scope to verify that the Data is shifted out on the negative edge of Clock. Capture scope traces with a picture and attach to the Test Record.

This completes the Data Phase Command section of the procedure. Record the successful completion of this test in the Test Record at the end of this procedure.

9.0 HVBS Connector Checks and Circuit Check-Outs

The pin connections for the two 79 pin circular connectors JP1 and JS2 are listed in Appendix 7. The pin connections for the two 9 pin MDM connectors to the High Voltage Bias Supplies are listed in Appendix 6.

9.1 Test of the HVBS DAC Commands, DAC Buffer, and Differential Drivers

To verify the operation of the HVBS DAC and Differential Driver make the following measurements. Verify that HVBS DAC is set to 0. Note: The commonality of the JHV1 and JHV2 connectors was measured during the initial voltage checks earlier in the procedure.

The reference for these measurements is the Lepracon connector shell.

This portion of the test may be omitted at the discretion of the Test Conductor.

Meas. No.	FREE Circuit Card Probe Point	Expected Voltage (+/- 50 mV)	Measured Voltage
1	TPREF1	1.25V	
2	TPDAC2	0V	
3	JDAC2	1.40V	
4	TPDAC3	2.50V	
5	JDAC1	0V	
6	TPDAC4	0V	
7	UDAC1D-14 (VREF)	2.50V	
8	JHV1-4 (HV-DACP)	1.40V	
9	JHV1-9 (HV-DACN)	1.40V	

The HVBS_Level_Wr command and Use_HV_Nominal_Wr command to change the DAC setting as shown to verify the linearity of the circuit.

This test may be automated using the LabView GSE via the [GARC HVBS DAC Level Test.txt](#) script.

The JDAC1 measurement for this section of the test may be omitted at the discretion of the Test Conductor.

Meas. No.	DAC SETTING	JHV1-4 (HV-DACP)	JHV1-9 (HV-DACN)	JDAC1 (DAC VOLTAGE)
1	000			
2	200			
3	400			
4	600			
5	800			
6	1000			
7	1200			

8	1400			
9	1600			
10	1800			
11	2000			
12	2200			
13	2400			
14	2600			
15	2800			
16	3000			
17	3200			
18	3400			
19	3600			
20	3800			
21	4000			
22	4095			

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

9.2 Test of the HVBS Triple Modular Redundancy Circuitry

This section tests the proper functioning of the GARC HVBS enable circuitry. Each pattern in the TMR logic will be tested to verify proper recovery from a single event upset. The GARC HV_ENABLE_1 pin is 185 and the HV_ENABLE_2 pins is 186. A truth table for proper TMR circuitry function is detailed below.

This test may be automated using the LabView GSE via the [GARC HV Enable Test.txt](#) script.

Enable Bit A	Enable Bit B	Enable Bit C	HV Enable Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

To verify the Enable command connect volt meters at JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) of the FREE board. Exact voltages for command on and off will be measured at the end of this section. For nominal power supply voltages, the nominal “ON” voltage is approximately 3.2V and “OFF” is approximately 0.015V. Reference the meter to the Lepracon connector body.

1. Send the GARC_Mode_Wr command with a data argument of 768 and verify the data with the GARC_Mode_Rd command.
2. Send the GARC_Status command. The data field in the return data stream should show that bits 1 and 2 are 0, indicating that HVBS 1 and 2, respectively, are disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.

3. Send the GARC_Mode_Wr command with decimal argument 770 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. . The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.
4. Send the GARC_Mode_Wr command with decimal argument 772 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.
5. Send the GARC_Mode_Wr command with decimal argument 774 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. . The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.
6. Send the GARC_Mode_Wr command with decimal argument 776 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. . The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
7. Send the GARC_Mode_Wr command with decimal argument 778 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. . The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
8. Send the GARC_Mode_Wr command with decimal argument 780 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.
9. Send the GARC_Mode_Wr command with decimal argument 782 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.
10. Send the GARC_Mode_Wr command with decimal argument 784 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
11. Send the GARC_Mode_Wr command with decimal argument 800 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
12. Send the GARC_Mode_Wr command with decimal argument 816 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
13. Send the GARC_Mode_Wr command with decimal argument 832 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
14. Send the GARC_Mode_Wr command with decimal argument 848 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.

15. Send the GARC_Mode_Wr command with decimal argument 864 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
16. Send the GARC_Mode_Wr command with decimal argument 880 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
17. Send the GARC_Mode_Wr command with decimal argument 782 and verify the data with the GARC_Mode_Rd command. Measure the voltage at the two HV_ENABLE pins:
 - a. HV_ENABLE_1 voltage JHV1-5: _____ (expected ~ 3.2V)
 - b. HV_ENABLE_2 voltage JHV2-5: _____ (expected ~ 3.2V)
18. Send the GARC_Mode_Wr command with decimal argument 768 and verify the data with the GARC_Mode_Rd command. Measure the voltage at the two HV_ENABLE pins:
 - a. HV_ENABLE_1 voltage JHV1-5: _____ (expected ~ 0.015V)
 - b. HV_ENABLE_2 voltage JHV2-5: _____ (expected ~ 0.015V)
19. Send the GARC_Reset command. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.

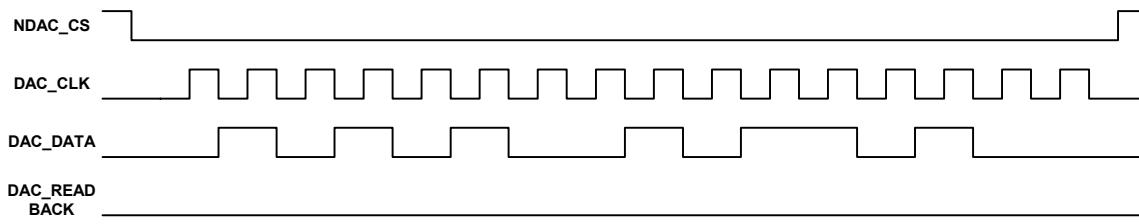
This completes the test of the HVBS enable/disable TMR circuitry. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

9.3 Capture of the DAC Control Signals

This section tests the proper commanding of the MAX5121 DAC. A voltmeter will be used to monitor the DAC output on the board under test.

This test may be omitted at the discretion of the Test Conductor.

1. Send the HVBS_Level_Wr command with a data argument of hex A5A (decimal 2650). Send the HVBS_Level_Rd command to verify.
2. Check that the scope is armed and then send the Use_HV_Nominal_Wr command. The scope should trigger and the following waveform should be displayed. Send the command twice the DAC_Read Back signal should be the same as the DAC_Data except it will be delayed one clock cycle. Verify that the DAC clock is nominally 5 MHz _____ (check)
3. Monitor the NDAC_CS signal (RDA21) and verify the waveform in step 7.
4. Monitor the DAC_CLK signal (RDA31) and verify the waveform in step 7.
5. Monitor the DAC_DATA signal (RDA30) and verify the waveform in step 7.
6. Monitor the DAC_READBACK signal (RDA26) and verify the waveform in step 7.
- 7.



DAC DATA WRITE WITH DATA PATTERN HEX A5A

8. Check that the scope is armed and then send the Use_HV_Nominal_Rd command. The software readback should capture the following value in the 16 bit return word: hex F4B4 (decimal 31348).
9. Move the probe on channel 1 to NDAC_CLR. Verify the scope is armed and send the GARC_Reset command. The scope should trigger and a valid active low clear signal should be observed on the scope.
 - a. Duration of the RESET pulse: _____ (expected ~ 150 ns)

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

9.4 Test of the SAA/HV Normal Modes

This section tests the proper functioning of the SAA/HV Normal modes.

1. Send the HVBS_Level_Wr command with a data argument of decimal 2048. Send the HVBS_Level_Rd command to verify the write command.
2. Send the SAA_Level_Wr command with a data argument of decimal 1024. Send the SAA_Level_Rd command to verify.
3. Using a multimeter at the JHV1 pin 4 connector, verify the HV_DACP voltage is 1.4V.
Value observed: _____
4. Send the Use_HV_Nominal command. Verify that the HV_DACP voltage is 2.1V.
Value observed: _____
4. Send the DAC_HVReg_Rd command and verify the return data pattern from the MAX5121 DAC is decimal 10240.
Value observed: _____
5. Send the Use_SAA_Level command. Verify that the HV_DACP voltage is 1.8V.
Value observed: _____
6. Send the DAC_SAAReg_Rd command and verify the return data pattern from the MAX5121 DAC is decimal 9216.
Value observed: _____
7. Send the GARC_Reset command. Verify that the HV_DACP voltage is 1.4V.
Value observed: _____
9. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

10.0 Characterizations of the FREE Assembly In-Rush Currents

This test will be used to characterize the transient currents associated with power-on for each FREE assembly. This test will require a current probe connected to an oscilloscope. This test is useful for characterizing the ACD electronics assembly. A fully populated FREE card and both ACD interface connectors connected is required to obtain an accurate measurement. Since the phototube signals are AC coupled to the system and provide essentially no load to the FREE card, these inputs need not be connected for this test.

Breakout boxes may be in place for this test and all pins shall be inserted into the break-out boxes except the following:

JP1 – 1, 3, 4 (ACD_VDD) and JP1 – 5, 7 (ACD_28V).
JP2 – 1, 3, 4 (ACD_VDD) and JP2 – 5, 7 (ACD_28V).

Place jumper wire loops in the BOB at pins JP1-1 and JP1-5 to measure the +3.3V and +28V in-rush currents, respectively.

This test may be omitted at the discretion of the Test Conductor.

Set the oscilloscope to trigger on the current probe. Place the current probe on the JP1-1 wire. Turn on the ACD electronics and capture the in-rush waveform (repeat this measurement until the full time and amplitude are correctly captured). Attach a printout of the in-rush plot to the Test Results Record of this procedure.

Move the current probe to the JP1-5 wire and reset the oscilloscope to trigger on the current probe. Turn on the ACD electronics and capture the in-rush waveform (repeat this measurement until the full time and amplitude are correctly captured). Attach a printout of the in-rush plot to the Test Results Record of this procedure. This current should be 0mA as no HVBS is connected.

Label the copies of the in-rush current plots with the test number, date, and test conductor name before continuing. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.0 FREE Verification Measurements Requiring an Oscilloscope and Multimeter

This section continues the verification of the FREE circuit card assembly. The measurements in this section require manual intervention due to the necessity for a measurement with the oscilloscope and/or multimeter.

11.1 GARC Test Pin Mux Verification

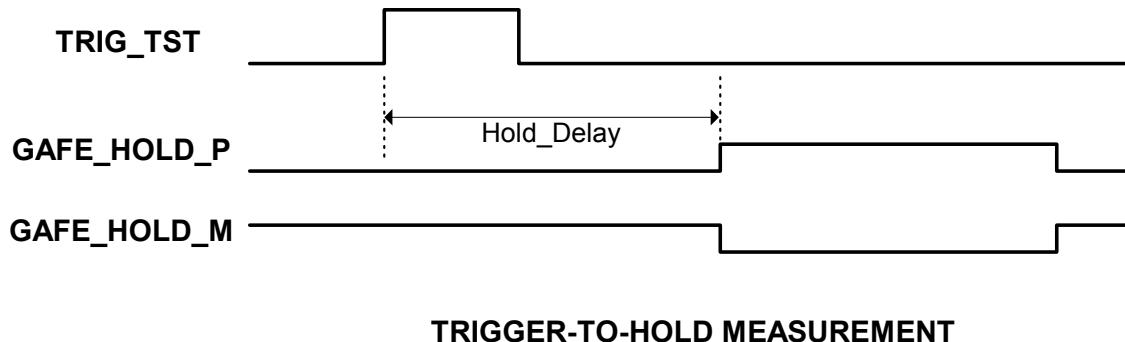
This section tests the proper functionality, switch the GARC test pin between the “Live” and “HitMap Test” outputs.

This test may be omitted at the discretion of the Test Conductor.

1. Send the GARC_Mode_Wr command with a data argument of 1792 to switch the GARC test pin mux to view the “live” signal. Send the GARC_Mode_Rd command to verify the register data. When configuration commands are sent, the “live” signal should go inactive low during the state machine busy time. This may be verified via the oscilloscope. The GARC test pin is pin 179 (TP179).
2. Send the GARC_Mode_Wr command with a data argument of 768 to switch the GARC test pin mux to view the “HitMap test” signal. Send the GARC_Mode_Rd command to verify the register data. When trigger commands are sent, the “HitMap test” signal should go active high during times when there is a delayed VETO signal present at the DISC_IN input. This may be verified via the oscilloscope. The GARC test pin is pin 179 (TP179).
3. Send the GARC_Reset command to ensure all registers are at the proper initial value. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.2 Test of the Hold Delay Operation

This section tests the proper functioning of the adjustment of the commandable delay function of the trigger to shaping amplifier hold signal. The trigger signal may be monitored on the GARC at pin 180 (TP180), TRIG_TST (GARC test board J7-9). The Hold signal may be monitored differentially on the GARC, GAFE_HOLD_P at pin 160 and GAFE_HOLD_M at pin 161, as shown in the diagram below. GAFE_HOLD may be measured across RT3.



This test may be omitted at the discretion of the Test Conductor.

1. Measure the DC levels of both GAFE_HOLD_P and GAFE_HOLD_M at RT3 and record the values below:

- a. GAFE_HOLD_P (DC) : _____ (expected ~ 870 mV)
 - b. GAFE_HOLD_M (DC): _____ (expected ~1600 mV)
2. Send the Hold_Delay_Wr command with a data argument of decimal 0 and verify with the Hold_Delay_Rd command. The Hold_Delay is variable with arguments of 0 – 127, representing 50 – 6400 ns.

The LabView test script **GARC Hold Delay Test.txt** may be used to partially automate this test.

Hold Delay Command	Measured Hold Delay (ns)	Expected Hold Delay (ns)
0		50
1		100
2		150
3		200
4		250
5		300
6		350
7		400
8		450
9		500
10		550
11		600
12		650
13		700
14		750
15		800
16		850
17		900
18		950
19		1000
20		1050
21		1100
22		1150
23		1200
24		1250
25		1300
26		1350
27		1400
28		1450
29		1500
30		1550
31		1600
32		1650
33		1700
34		1750
35		1800
36		1850
37		1900
38		1950
39		2000
40		2050
41		2100
42		2150
43		2200

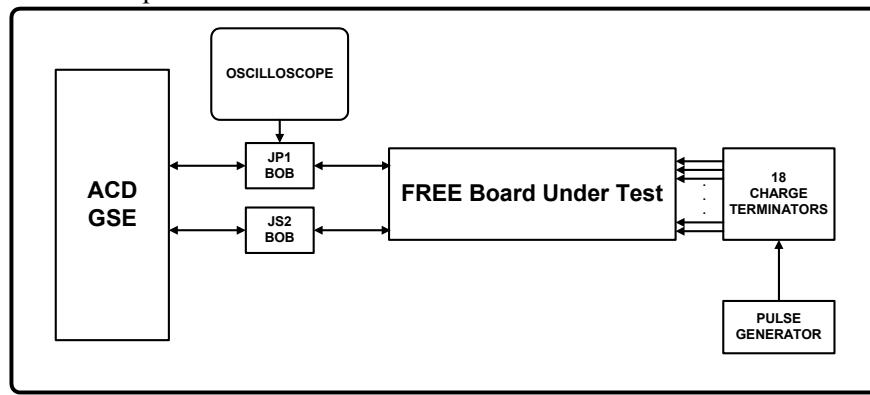
44		2250
45		2300
46		2350
47		2400
48		2450
49		2500
50		2550
51		2600
52		2650
53		2700
54		2750
55		2800
56		2850
57		2900
58		2950
59		3000
60		3050
61		3100
62		3150
63		3200
64		3250
65		3300
66		3350
67		3400
68		3450
69		3500
70		3550
71		3600
72		3650
73		3700
74		3750
75		3800
76		3850
77		3900
78		3950
79		4000
80		4050
81		4100
82		4150
83		4200
84		4250
85		4300
86		4350
87		4400
88		4450
89		4500
90		4550
91		4600
92		4650
93		4700
94		4750
95		4800
96		4850
97		4900
98		4950
99		5000

100		5050
101		5100
102		5150
103		5200
104		5250
105		5300
106		5350
107		5400
108		5450
109		5500
110		5550
111		5600
112		5650
113		5700
114		5750
115		5800
116		5850
117		5900
118		5950
119		6000
120		6050
121		6100
122		6150
123		6200
124		6250
125		6300
126		6350
127		6400

3. Send the Hold_Delay_Wr command with a data argument of 0. Verify the command using the Hold_Delay_Rd readback.
4. Send the GARC_Reset command to restore all register values to their initial state. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.3 Test of the AEM VETO Signal Functionality

This section tests the proper functioning of the adjustment of the commandable delay function of the trigger to shaping amplifier hold signal. The trigger signal may be monitored on the GARC at pin 180 (TP180). This section tests the proper functioning of the commandable functions of the AEM_VETO signals. This test requires the use of an oscilloscope, a tail pulse generator for input stimulus, and test points to monitor the AEM_VETOs. The test setup is as shown below.

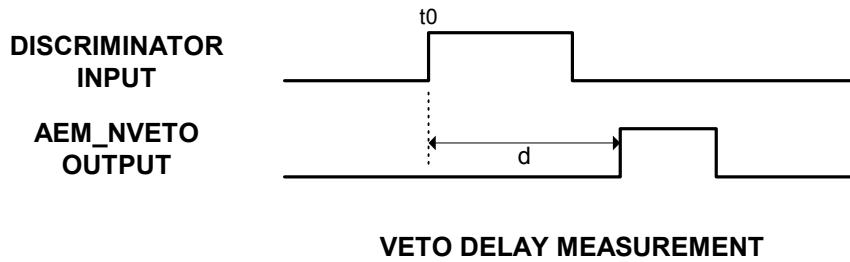


GARC VETO Test Setup

All 18 of the Charge Terminator Capacitors are tied together to the output of the test pulser for this portion of the test. The input test rate should be set at approximately 60 Hz. The oscilloscope probe will be monitoring the 18 AEM_VETO outputs. Between commands, this probe will be moved manually from test point to test point to perform this test. Setting the scope to acquire on the pulse output, this test will be measuring the delay (time from trigger to VETO leading edge) and width (time between leading and trailing edges) of each of the VETO pulses. Since each input has the same signal, the outputs should also be common in delay and width. In timing measurements, the activation signal from the test pulser will be the relative zero.

11.4 Veto Delay Test

1. The input is a tail pulse into the FREE board and the outputs are on the AEM Simulator GSE board or the JP1/JS2 connector. For this measurement, it may be convenient to use the oscilloscope in the “persist” mode and then monitor the minimum delay. This test may be automated using the LabView GSE via the script **GARC_VETO_Delay_Test.txt**.
2. Send the Veto_Delay_Wr command with a data argument of 0. Confirm this command via the Veto_Delay_Rd command.
3. Send the Veto_Width_Wr command with a data argument of 0. Confirm this command via the Veto_Width_Rd command. Using the oscilloscope, measure the delay from scope trigger to leading edge of VETO for each of the 18 pulses and record the data in the table below. Note that all 18 pulses are designed to have identical timing for this test. The VETO Delay is the time **d** in the diagram below.



VETO DELAY MEASUREMENT

Measure from the peak of the Tail Pulse to the AEM GSE Veto Signal. The amplitude of the tail pulse signal should be around 1V to remove the rise time jitter on the discriminator.

4. Repeat the Veto_Delay_Wr, Veto_Delay_Rd sequence for data argument values of decimal 1 to 31. Record the results in the table below. Note that there is a 50 ns jitter on each of the “expected” numbers.

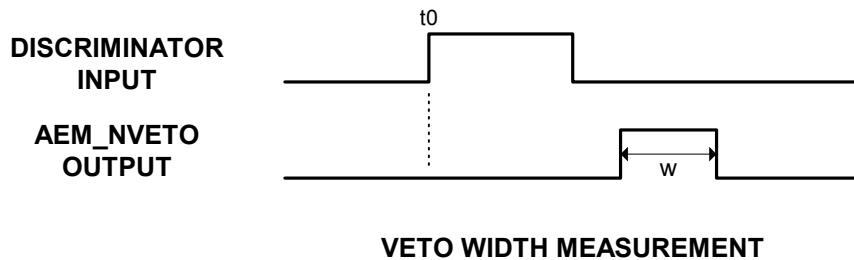
Veto_Delay Setting	Delay from Scope trigger to Leading Edge (ns)	Expected (ns)
0		300
1		350
2		400
3		450
4		500
5		550
6		600
7		650
8		700
9		750
10		800
11		850
12		900
13		950
14		1000
15		1050

16		1100
17		1150
18		1200
19		1250
20		1300
21		1350
22		1400
23		1450
24		1500
25		1550
26		1600
27		1650
28		1700
29		1750
30		1800
31		1850

5. Send the Veto_Delay_Wr command with a data argument of 0 and a Veto_Delay_Rd command to verify this value. Make a picture of the Tail pulse signal, veto out of the GAFE and the veto at out of the AEM.
Picture file name- _____
6. Repeat measurement for all channels.
7. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.5 Veto Width Test

1. The setup for this test is the same as the VETO Delay test above. This test may be automated using the LabView GSE via the GARC VETO Width Test.txt script.
2. Send the Veto_Width_Wr command with a data argument of 0. Confirm this command via the Veto_Width_Rd command. Using the oscilloscope, measure the width of each of the 18 VETO pulses and record the data in the table below. Note that the width of each of these pulses is expected to be identical for any given commanded setting. The VETO Width is the “w” parameter in the diagram below.



3. Repeat the Veto_Width_Wr, Veto_Width_Rd sequence for data argument values of decimal 1 to 7. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

Veto Width	Measured Width of VETO Pulse (ns)	Expected Width (ns)
0		50
1		100
2		150
3		200
4		250
5		300
6		350
7		400

11.6 Veto Enable and Disable Test

This test may be automated when using the LabView GSE via test script **GARC VETO Disable A/B SideTest.txt**. Monitor the counters to verify the Veto signals. Reference the meter to the Lepracon Connectors body.

- Send the GARC_Mode_Wr command with the value of 768 to enable the “A” and enable the “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 768. Generate a TCI event and measure the Veto amplitude swing at the JP1-71 and JS2-71 connectors for Channel 0 for both A and B.

JP1-71 - _____ (expected 400mV)

JS2-71 - _____ (expected 400mV)

- Send the GARC_Mode_Wr command with the value of 512 to disable the “A” and enable the “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 512. Generate a TCI event and measure the Veto amplitude swing at the JP1-71 and JS2-71 connectors for Channel 0 for both A and B.

JP1-71 - _____ (expected 50mV)

JS2-71 - _____ (expected 400mV)

- Send the GARC_Mode_Wr command with the value of 256 to enable the “A” and disable the “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 256. Generate a TCI event and measure the Veto amplitude swing at the JP1-71 and JS2-71 connectors for Channel 0 for both A and B.

JP1-71 - _____ (expected 400mV)

JS2-71 - _____ (expected 50mV)

- Send the GARC_Mode_Wr command with the value of 0 to disable both the “A” and “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 0. Generate a TCI event and measure the Veto amplitude swing at the JP1-71 and JS2-71 connectors for Channel 0 for both A and B.

JP1-71 - _____ (expected 50mV)

JS2-71 - _____ (expected 50mV)

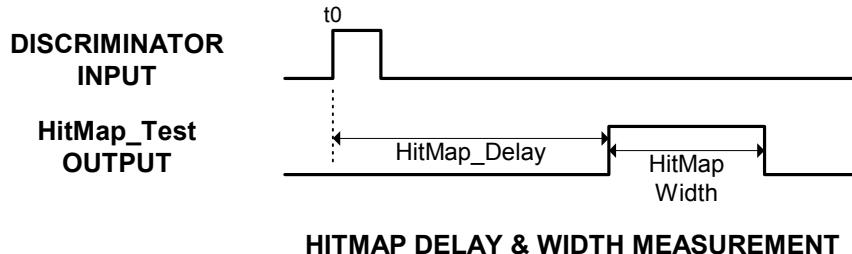
- Send the GARC_Mode_Wr command with the value of 256 to enable the “A” and disable the “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 256.
- Send the VETO_En0_Rd command and verify that the return data has value ‘hFFFF (65535). Send the VETO_En1_Rd command and verify that the return data has the value 3

7. Send the VETO_En0_Wr command with a data argument ‘hFFFE (65534). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 0.
8. Send the VETO_En0_Wr command with a data argument ‘hFFFD (65533). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 1.
9. Send the VETO_En0_Wr command with a data argument ‘hFFFB (65531). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 2.
10. Send the VETO_En0_Wr command with a data argument ‘hFFF7 (65527). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 3.
11. Send the VETO_En0_Wr command with a data argument ‘hFFEF (65519). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 4.
12. Send the VETO_En0_Wr command with a data argument ‘hFFDF (65503). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 5.
13. Send the VETO_En0_Wr command with a data argument ‘hFFBF (65471). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 6.
14. Send the VETO_En0_Wr command with a data argument ‘hFF7F (65407). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 7.
15. Send the VETO_En0_Wr command with a data argument ‘hFEFF (65279). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 8.
16. Send the VETO_En0_Wr command with a data argument ‘hFDFF (65023). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 9.
17. Send the VETO_En0_Wr command with a data argument ‘hFBFF (64511). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 10.
18. Send the VETO_En0_Wr command with a data argument ‘hF7FF (63487). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 11.
19. Send the VETO_En0_Wr command with a data argument ‘hEFFF (61439). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 12.
20. Send the VETO_En0_Wr command with a data argument ‘hDFFF (57343). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 13.
21. Send the VETO_En0_Wr command with a data argument ‘hBFFF (49151). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 14.

22. Send the VETO_En0_Wr command with a data argument ‘h7FFF (32767). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 15.
23. Send the VETO_En0_Wr command with a data argument ‘hFFFF (65535). Verify the command with the VETO_En0_Rd command. Generate a TCI event for all channels and verify that all VETOs are on.
24. Send the VETO_En1_Wr command with a data argument 2. Verify the command with the VETO_En1_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 16.
25. Send the VETO_En1_Wr command with a data argument 1. Verify the command with the VETO_En1_Rd command. Generate a TCI event for all channels and verify that all VETOs are on with the exception of channel 17.
26. Send the GARC_Mode_Wr command with the value of 512 to Disable the “A” and enable the “B” side VETOs. Send the GARC_Mode_Rd command and verify that the return data has a value of 512. Repeat steps 6 to 25 and verify the B side functionality.
27. Send the GARC_Reset command to restore all register values to their initial state. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.7 Test of Hit Map Functionality

This section tests the proper functioning of the commandable functions of the HitMap test point. This test requires the use of an oscilloscope, a tail pulse generator for input stimulus, and test points to monitor the AEM_VETOs. The test setup is identical to the VETO test setup shown above. Only channel 00 is available on the test pin for HitMap verification. The diagram below details the measurement points to use with the digitizing oscilloscope.



11.8 HitMap Width Test

This test may be automated using the LabView GSE via the [GARC_HitMap_Width_Test.txt](#) script.

This test may be omitted at the discretion of the Test Conductor.

1. Send the HitMap_Deadtime_Wr command with a data argument of 0. Verify this command with the HitMap_Deadtime_Rd command.
2. Send the GARC_Mode_Wr command with a data argument of decimal 768 to ensure the test pin multiplexer is set to the HitMap_Test output. Place an oscilloscope probe on this test point (TP179).
3. Send the HitMap_Width_Wr command with a data argument of 0. Verify the command using the HitMap_Width_Rd readback.

4. Send the HitMap_Delay_Wr command with a data argument of 0. Verify the command using the HitMap_Delay_Rd readback.
5. Send the HitMap_Deadtime_Wr command with a data argument of 0. Verify the command using the HitMap_Deadtime_Rd readback.
6. Set up the test pulser to stimulate the discriminator input for channel 0. Monitor the HitMap Test output with the oscilloscope triggered from the test pulser. Using the HitMap_Width_Wr command with data arguments of 0 – 15, verify the HitMap Width varies as expected and record the data in the table below.

HitMap Width Command	Measured Width (ns)	Expected Width (ns)
0		150
1		200
2		250
3		300
4		350
5		400
6		450
7		500
8		550
9		600
10		650
11		700
12		750
13		800
14		850
15		900

7. Send the HitMap_Width_Wr command with a data argument of 0 to reset the HitMap Width. Verify the command with the HitMap_Width_Rd command.
8. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.9 HitMap Delay Test

This setup is the same as the previous section with the exception that the oscilloscope is in persistence mode and the trigger is on the discriminator input. The minimum delay is the number to be recorded. This test may be automated using the LabView GSE via the GARC HitMap Delay Test.txt script.

This test may be omitted at the discretion of the Test Conductor.

1. Using the HitMap_Delay_Wr command with data arguments of 0 – 31, verify the HitMap Delay varies as expected and record the data in the table below.

HitMap Delay Command	Measured Delay (ns)	Expected Delay (ns)
0		900
1		950
2		1000
3		1050
4		1100
5		1150
6		1200
7		1250
8		1300
9		1350
10		1400
11		1450
12		1500
13		1550
14		1600
15		1650
16		1700
17		1750
18		1800
19		1850
20		1900
21		1950
22		2000
23		2050
24		2100
25		2150
26		2200
27		2250
28		2300
29		2350
30		2400
31		2450

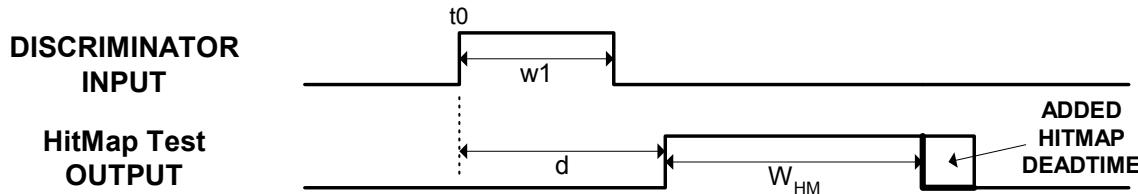
2. Send the HitMap_Delay_Wr command with a data argument of 0 to reset the HitMap Delay. Verify the command with the HitMap_Delay_Rd command.
3. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.10 HitMap Deadtime Stretch Test

This test will monitor the function of the HitMap_Deadtime adjustment. This Deadtime register adds a time (0 to 350 ns) to the end of the HitMap pulse, starting at the end of the HitMap Width calculation. The diagram below illustrates the position of the added time window.

This test may be automated using the LabView GSE via [the GARC HitMap Deadtime Test.txt](#) script. .

This test may be omitted at the discretion of the Test Conductor.



HITMAP DEADTIME TEST

1. Using the HitMap_Deadtime_Wr command with data arguments of 0 – 7, verify the HitMap Deadtime extends the trailing edge of the HitMap test pulse as expected and record the data in the table below.

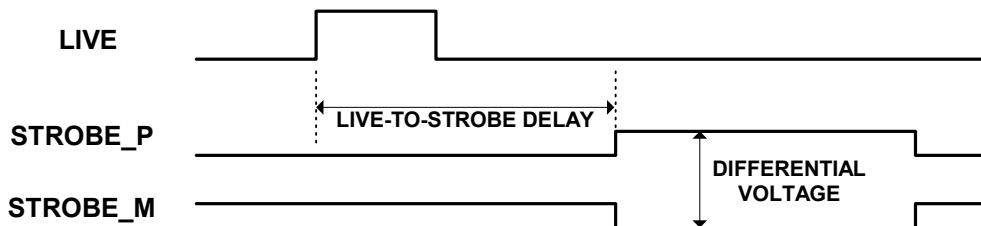
HitMap Deadtime Command	Measured Deadtime Pulse Extension - (ns)	Expected Deadtime Pulse Extension -(ns)
0		0
1		50
2		100
3		150
4		200
5		250
6		300
7		350

2. Send the GARC_Reset command to restore all register values to their initial state.
3. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.11 Strobe Test

This section tests the proper functioning of the commandable strobe pulse to the GAFEs from the GARC. This signal is used as a level command to the GAFE(s) to indicate the timing of the test charge injection to the amplifier front end. Using the oscilloscope monitoring Live on GARC pin 179 (TP179), GAFE_STROBEP on GARC pin 163 and GAFE_STROBEM on GARC pin 164 (RT4), perform the following (as shown in the diagram below):

This test may be omitted at the discretion of the Test Conductor.



STROBE COMMAND TEST

1. Send the ADC_TACQ_Wr command with a variable of 0. Verify command with a ADC_TACQ_Rd command.

2. Measure the DC levels of both STROBE_P and STROBE_M and record the values below
 - a. STROBE_P (DC): _____ (expected ~ 700 mV)
 - b. STROBE_M (DC): _____ (expected ~1600 mV)
3. Send the GARC_Mode_Wr command with data argument 1792 to switch the test pin multiplexer to the Live signal.
4. Set the scope to acquire on the negedge of Live. Send the GARC_Cal_Strobe command (this is a dataless command so the data argument is 0).
5. Verify the STROBE command has executed by noting the differential signal on the two oscilloscope channels. It is expected that the voltage amplitude of each side of the differential is greater than 50 mV and that the pulse duration is approximately 10 μ sec.

STROBEP to STROBEM differential voltage: _____ (expected 900 mV)

Live-to-STROBE delay: _____ (expected ~ 150 ns)

STROBE pulse duration (μ sec): _____ (expected 12.5 μ sec)

6. Send the GARC_Reset command to restore all register values to their initial state.
7. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.12 Capture of the ADC Control Signals

This test may be omitted at the discretion of the Test Conductor.

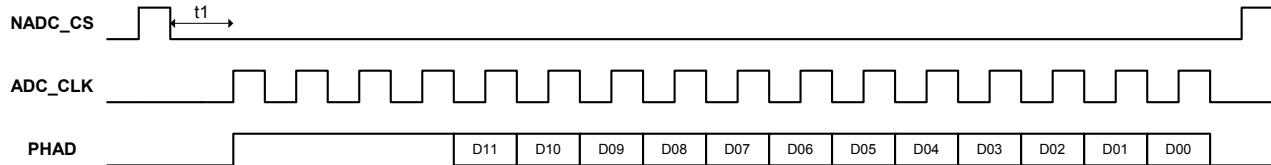
1. Connect the probe to ADC_CLK (RA3).
2. Send the TRIG_ZS command to initiate an analog-to-digital conversion. The scope should trigger and the following waveform should be displayed. Verify that the ADC clock is nominally 2 MHz at RA3.

Clock rate measured: _____ MHz

3. Measure the duration of the NADC_CS at RA6:

Duration _____ (expected ~ 10.6 μ sec)

4. The time t1 represents the total ADC TACQ (ADC acquisition time).



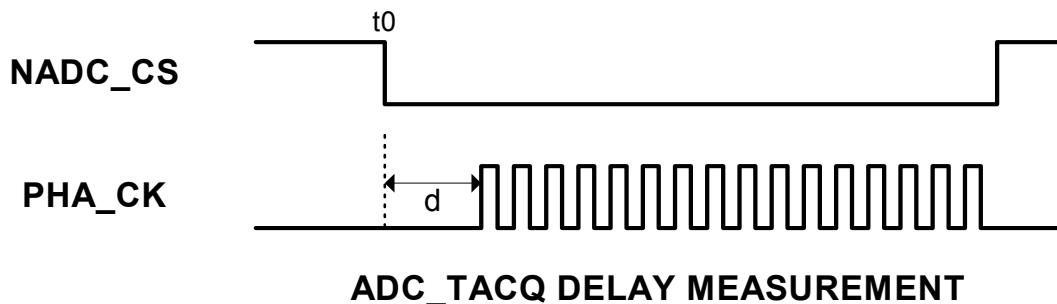
MAX145 ADC CONVERSION CYCLE

At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.13 ADC TACQ Test

This test may be omitted at the discretion of the Test Conductor.

- The next parameter to be measured will be the ADC time to acquisition (essentially the settling time allowed for the analog signal). This is a command with a 6 bit data argument. This alters the time between the ADC chip select transitioning active low and the start of the ADC clock. The register is set with the ADC_TACQ_Wr command and verified with the ADC_TACQ_Rd command. For each value of ADC_TACQ in the table below, record the time from the falling edge of the ADC_CS_N and the rising edge of the first ADC clock. Nominally, with an ADC_TACQ register setting of 0, there will be a CS \rightarrow PHA clock delay time of 2500 ns. There is the potential for a small amount of synchronization jitter (~few clocks) within the state machine on this parameter.



For each ACD_TACQ step, measure the delay, **d**, as shown in the diagram above. For the table below, the important parameter is the even 50 ns spacing on each step from the original zero point.

This test may be automated using the LabView GSE script [GARC ADC TACQ Test.txt](#).

ADC TACQ Register	Measured Time CS \rightarrow PHA Clock (ns)	Expected Time CS \rightarrow PHA Clock (ns)
0		2850
1		2900
2		2950
3		3000
4		3050
5		3100
6		3150
7		3200
8		3250
9		3300
10		3350
11		3400
12		3450
13		3500
14		3550
15		3600
16		3650
17		3700
18		3750
19		3800
20		3850
21		3900
22		3950
23		4000

24		4050
25		4100
26		4150
27		4200
28		4250
29		4300
30		4350
31		4400
32		4450
33		4500
34		4550
35		4600
36		4650
37		4700
38		4750
39		4800
40		4850
41		4900
42		4950
43		5000
44		5050
45		5100
46		5150
47		5200
48		5250
49		5300
50		5350
51		5400
52		5450
53		5500
54		5550
55		5600
56		5650
57		5700
58		5750
59		5800
60		5850
61		5900
62		5950
63		6000

2. Send the GARC_Reset command to restore all register values to their initial state. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

11.14 Test of the GARC LVDS Circuitry Driver Currents

This test may be omitted at the discretion of the Test Conductor.

This section tests the proper functioning of the GARC LVDS Driver circuitry. It is required that all LVDS drivers be terminated at the receiver with a 100 ohm resistor. The ACD-to-AEM nominal drive current is 3.5 mA across the 100 ohms for a voltage differential of 350 mV.

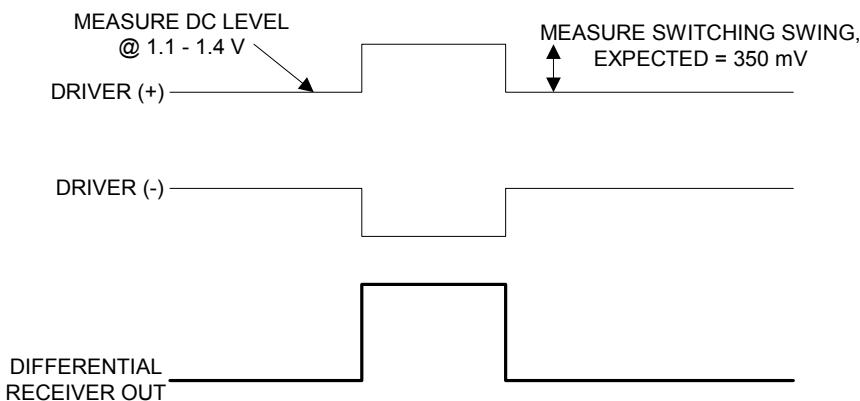
There are 6 LVDS receiver input pairs to the GARC:

- a) ACD_CLK_A, ACD_CLK_B
- b) ACD_CMD_A, ACD_CMD_B
- c) ACD_RESET_A, ACD_RESET_B

There are 40 LVDS driver output pairs from the GARC:

- d) ACD_NSDATA_A, ACD_NSDATA_B
- e) ACD_NVETO_nnA, ACD_NVETO_nnB (where nn is 00 – 17)
- f) ACD_CNO_A, ACD_CNO_B

The “A” side interface will be examined first. Verify that an AEM (or AEM simulator) is connected to the GARC “A” side interface. Using a digitizing oscilloscope, measure the DC baseline and switching differential voltage on each of the driver/receiver pairs. Two scope probes may be used, one on each side of the differential receiver inputs. The DC level and switching voltages may be measured as diagrammed below. The measurement will be made with the Drivers enabled and with them disabled.



Remove the Breakout Box on JP1 and JS2 and record the information for each pin on the AEM Simulator in the table below. Please document the data from the following steps in the copy of the Comprehensive Performance Test Record associated with this procedure.

Obtain a scope picture of the nominal pulse Amplitude Swings

GARC Signal	Signal Location	- DC Level (V) Enabled	+ DC Level (V) Disabled	- DC Level (V) Enabled	+ DC Level (V) Disabled
ACD_NVETO_12B	R1				
ACD_NVETO_12A	R2				
ACD_NVETO_11B	R3				
ACD_NVETO_11A	R4				
ACD_NVETO_10B	R5				
ACD_NVETO_10A	R6				
ACD_NVETO_09B	R7				
ACD_NVETO_09A	R8				
ACD_NVETO_08B	R9				
ACD_NVETO_08A	R10				
ACD_NVETO_07B	R11				
ACD_NVETO_07A	R12				
ACD_NVETO_06B	R13				
ACD_NVETO_06A	R14				
ACD_NVETO_05B	R15				
ACD_NVETO_05A	R16				
ACD_NVETO_04B	R17				

ACD_NVETO_04A	R18				
ACD_NVETO_03B	R19				
ACD_NVETO_03A	R20				
ACD_NVETO_02B	R21				
ACD_NVETO_02A	R22				
ACD_NVETO_01B	R23				
ACD_NVETO_01A	R24				
ACD_NVETO_00B	R25				
ACD_NVETO_00A	R26				
ACD_CNO_B	R27				
ACD_CNO_A	R28				
ACD_NVETO_13B	R31				
ACD_NVETO_13A	R32				
ACD_NVETO_14B	R33				
ACD_NVETO_14A	R34				
ACD_NVETO_15B	R35				
ACD_NVETO_15A	R36				
ACD_NVETO_16B	R37				
ACD_NVETO_16A	R38				
ACD_NVETO_17B	R39				
ACD_NVETO_17A	R40				
ACD_NSDATA_B	R29				
ACD_NSDATA_A	R30				

Measure the GAFE to GARC LVDS signals.

Obtain a scope picture of the nominal pulse Amplitude Swings

This test may be skipped at the discretion of the Test Conductor.

GARC Signal	GAFE "n" Pin	DC Level (V)	Switch Swing (V)
DISC_00	26		
CHID_00	25		
IRTN_00	24		
DISC_01	26		
CHID_01	25		
IRTN_01	24		
DISC_02	26		
CHID_02	25		
IRTN_02	24		
DISC_03	26		
CHID_03	25		
IRTN_03	24		
DISC_04	26		
CHID_04	25		
IRTN_04	24		
DISC_05	26		
CHID_05	25		
IRTN_05	24		
DISC_06	26		
CHID_06	25		
IRTN_06	24		
DISC_07	26		

CHID_07	25		
IRTN_07	24		
DISC_08	26		
CHID_08	25		
IRTN_08	24		
DISC_09	26		
CHID_09	25		
IRTN_09	24		
DISC_10	26		
CHID_10	25		
IRTN_10	24		
DISC_11	26		
CHID_11	25		
IRTN_11	24		
DISC_12	26		
CHID_12	25		
IRTN_12	24		
DISC_13	26		
CHID_13	25		
IRTN_13	24		
DISC_14	26		
CHID_14	25		
IRTN_14	24		
DISC_15	26		
CHID_15	25		
IRTN_15	24		
DISC_16	26		
CHID_16	25		
IRTN_16	24		
DISC_17	26		
CHID_17	25		
IRTN_17	24		

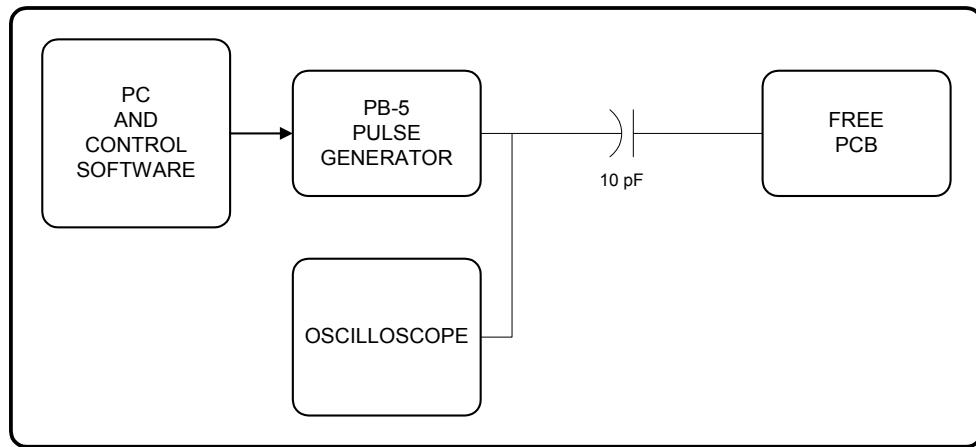
12.0 FREE Circuit Assembly Characterization Tests

The following tests utilized NIM-mounted laboratory pulse generators to simulate a phototube input at the GAFE inputs. Benchtop monitoring equipment will also be used. These tests will characterize the GAFE ASICs and associated readout circuitry. The VETO enable/disable function will be tested.

12.1 Characterization of each of the 18 GAFE chips

This test will verify the operation for each GAFE ASIC on the FREE printed circuit card. Included in this test will be the ADC conversion values as measured at the GARC. The low-energy threshold will be characterized during this test. The HLD enable/disable function will be tested.

A 10 pF charge terminator will be used for the each FREE board channel in the following setup.



In this case, the charge input to the FREE card is $Q = C \cdot V$, so 0.64 pC is approximately 64 mV on the scope.

Run the automatic characterization script to test the following

- 1) Register test
- 2) Bias DAC Test (LE)
- 3) Bias DAC Test (HE)
- 4) Hold Delay
- 5) INL Test (LE)
- 6) INL Test (HE)
- 7) Crossover point (LE/HE)
- 8) Hitmap Delay Test
- 9) Veto DAC Test
- 10) Vernier DAC Test
- 11) HLD DAC Test
- 12) TCI (LE)
- 13) TCI (HE)

All printouts are to be attached to the Test Results Record.

Settings being used for the following tests:

Create a configuration script for the FREE board under test.

File Name _____

GAFE Configuration

GAFE Channel	Mode	VETO DAC	VETO VERNIER	HLD DAC	BIAS DAC	TCI DAC
0						
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						

GARC Configuration

Register	Test Value
Veto_Delay	
HVBS_Level	
SAA_Level	
Hold_Delay	
Veto_Width	
HitMap_Width	

HitMap_Deadtime	
HitMap_Delay	
PHA_En0	
PHA_En1	
VETO_En0	
VETO_En1	
Max_PHA	
GARC_Mode	
FREE_Board_ID	
GARC_Version	
PHA_Threshold_00	
PHA_Threshold_01	
PHA_Threshold_02	
PHA_Threshold_03	
PHA_Threshold_04	
PHA_Threshold_05	
PHA_Threshold_06	
PHA_Threshold_07	
PHA_Threshold_08	
PHA_Threshold_09	
PHA_Threshold_10	
PHA_Threshold_11	
PHA_Threshold_12	
PHA_Threshold_13	
PHA_Threshold_14	
PHA_Threshold_15	
PHA_Threshold_16	
PHA_Threshold_17	
ADC_TACQ	

12.2 MUXSH DC Level versus BIAS Level

This test may be skipped at the discretion of the Test Conductor.

Set the GAFE Configuration Register for a PHA RANGE MODE bit = 1 (Auto Ranging off) and the RANGE SELECT bit = 0 (Low Range). Change the Bias level and measure each of the 18 GAFE MUXSH DC Levels. Repeat for RANGER SELECT bit = 1 (High Range)

GAFE Channel	BIAS 0 Low Range	BIAS 0 High Range	BIAS 2 Low Range	BIAS 2 High Range	BIAS 4 Low Range	BIAS 4 High Range	BIAS 6 Low Range	BIAS 6 High Range
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								
17								

12.3 VETO and ADC Crosstalk Test

This test may be skipped at the discretion of the Test Conductor.

The function of this portion of the test is to check for crosstalk in the digital sections of the FREE card and their connections to individual GAFE channels. For this test, the GAFE VETO thresholds will all be set based upon the settings from the characterization test in 12.1. With no signal connected to any of the GAFE channel inputs, configure the AEM simulator to send event triggers. While the system is doing analog-to-digital conversions, verify that there are no VETO signals coming from the FREE card. This verifies that the ADC conversions have an ADC-to-VETO crosstalk level below threshold. In the absence of an input pulse, this also provides the ADC zero energy baseline, which may be recorded in the table below.

Disconnect the pulser from the Charge Terminator box.

Record the ADC Baseline peak for each channel. Save the data file.

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

10	
11	
12	
13	
14	
15	
16	
17	

Data File name - _____

The next step is to verify that no Crosstalk exists on the board by putting a pulse into one GAFE channel at a time (pulse amplitude 1V into 10pF) and verify that the PHA baseline on adjacent channels is not noticeably affected. This needs to be performed serially for all 18 channels.

While the pulse is input to one channel at a time, it shall be verified that a VETO pulse is output for the channel receiving the input and that no other VETOes are generated. This verifies the absence of VETO to VETO crosstalk. Record confirmation in the table below.

GAFE Channel	Crosstalk Checked	Single VETO Verified
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		

12.4 Multiple System Clock Speed Test at +3.0V and +3.6V

This test may be Omitted at the discretion of the Test Conductor.

The function of this test is to verify operation of the FREE board circuitry over the range of allowable clock frequencies and Power Supply Rail limits. The majority of this test has been performed at the nominal 20 MHz clock and has therefore verified the nominal frequency. This portion of the test will verify operation at the low and high limit frequencies and at min and max rail voltages.

- 1) Set the Power Supply to +3.0V

+3.0V current - _____

- 2) Set the clock frequency to the 22 MHz high limit.
- 3) Run the register test from section 8.4
- 4) Run the test of the DAC interface circuitry, section 9.4
- 5) Run the ADC Baseline test of 12.5.
- 6) Set the Power Supply to +3.6V

+3.6V current - _____

- 7) Run the register test from section 8.4
- 8) Run the test of the DAC interface circuitry, section 9.4
- 9) Run the ADC Baseline test of 12.5.
- 10) Set the clock frequency to the 14 MHz low limit leave the power supply set to +3.6V.
- 11) Run the register test from section 8.4
- 12) Run the test of the DAC interface circuitry, section 9.4
- 13) Run the ADC Baseline test of 12.5.
- 14) Set the Power Supply to +3.0V
- 15) Run the register test from section 8.4
- 16) Run the test of the DAC interface circuitry, section 9.4
- 17) Run the ADC Baseline test of 12.5.

Reset the clock frequency to the 20 MHz nominal.

12.5 Power Supply Rail Tests – 3.0V to 3.6V

Power supply rail voltage testing has been performed on both the GARC and GAFE ASICs prior to integration to the FREE card assembly. This test will verify the operation of the card at the upper and lower voltage limits of +3.60V and +3.00V, respectively. This test will repeat sections performed previously in this test, comparing the results.

Set the power supply to +3.6V.

Run the GAFE Characterization Test Section 12.1

Record the Data File name - _____

Set the power supply to +3.0V.

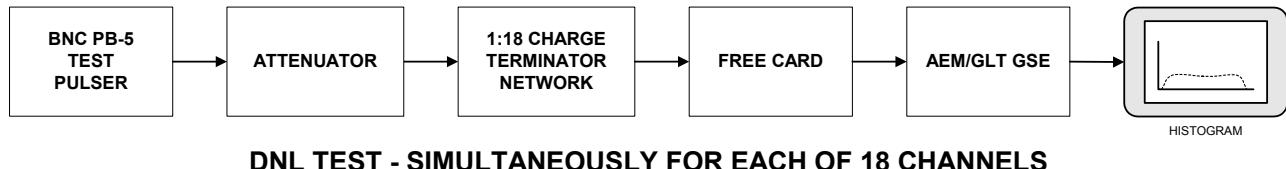
Run the GAFE Characterization Test Section 12.1

Record the Data File name - _____

12.6 Differential Non-Linearity (DNL) Test

This test may be omitted at the discretion of the Test Conductor.

This test will monitor the DNL of each GAFE and ADC pair over the low-energy range. Differential Non-Linearity is used to describe the deviations between the measure and the ideal 1 LSB change of transition voltages in the ADC's transfer characteristic. The code width of the converter represents the span of input voltage which results in a given quantization level. This is a measure of the local slope error of the converter. The setup is shown below.



DNL TEST - SIMULTANEOUSLY FOR EACH OF 18 CHANNELS

The differential non-linearity test is performed by sweeping the input pulse through the entire ADC dynamic range. A statistical analysis on ADC bin width is performed. For this test, we will 0 – 10 MIP equivalents for the GAFE Low Range.

The pulser should be set for a fast rise time, a long fall time, and a repetition rate of approximately 1 kHz. The amplitude should be set to the ramp mode with a maximum amplitude pulse of approximately 7 pC, or about 700 mV into a 10 pF charge terminator. This test should be run until there are approximately 1000 counts per channel in the main portion of the histogram. At the end of the test, the DNL may be calculated for 11 bits as

$$DNL(\%) = \left(\frac{T_{n+1} - T_n}{V_{FS}/2^{11}} - 1 \right) * 100\%$$

Where T_n is the transition voltage of the n^{th} quantization level. For the ACD FREE electronics, it is desirable that we demonstrate no missing codes to the 11 bit level.

Data file name - _____

END OF COMPREHENSIVE PERFORMANCE TEST

Appendix 1: GARC Documentation

A more complete set of documentation (such as the Verilog, EDIF, layout, and wirebonding diagram) is available on the LHEA ACD electronics web page at:

<http://lhea-glast.gsfc.nasa.gov/acd/electronics/#garc>

Appendix 2: FREE Circuit Card Test Points

The FREE circuit card assembly has the following test point locations available for use during circuit-card level testing.

Schematic Page	FREE Card Test Point	Location	Near Part, Pin	Expected Value	Notes
3	Op Amp Ground	TPDAC4	UDAC1-8	~ 200 mV	Limited due to (-) rail
3	REFTST	TPDAC3	UDAC1-1	2.5	1.25V ref x 2
3	DAC Output	TPDAC2	UDAC3-2	0 – 1.249 V	Commandable DAC Output
3	DAC reference	TPREF1	UDAC3-14	1.25 V	Internal DAC Reference
3	DAC Receiver Test	JDAC1	UDAC1-7	HVP - HVN	Differential Receiver as in HVBS
3	Differential Driver Offset	JDAC2	UDAC2-7	~ 1.40V	HVP, HVN offset for DAC differential drivers
6	+3.3 V before CM choke	LCM1-1	LCM1-1	+3.3 V	FREE board voltage prior to filtering
6	+3.3 V digital	CP2-1	CP3-1	+3.3 V	FREE board voltage VDD after CM choke
6	+3.3 V analog	CP7-1	CP8-1	+3.3 V	FREE board voltage VCC after filtering
7	LVDS PRESET ADJ	RG10-1	GARC-184		
7	BIAS_DRV_H	RG3-1	GARC-160		
7	BIAS_DRV_L	RG1-1	GARC-169		
7	BIAS_RCVR	RG6-1	GARC-156		
7	HLD_WOR_BIAS	RG8-1	GARC-104		
7	HITMAP TEST	TG179	GARC-179		GARC Trigger Test Point
7	TRIG TEST	TG180	GARC-180		GARC HitMap Test Point
7	VETO_ENA_TEST	TG183	GARC-183		GARC Veto Enable A Status Test Point
7	GARC Core Voltage	CG9-1	CG8-1	+3.2 V	GARC VDD
9	FREE ID, Bit 0	RIL0-1	UID1-11	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 1	RIL1-1	UID1-12	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 2	RIL2-1	UID1-13	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 3	RIL3-1	UID1-14	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 4	RIL4-1	UID1-3	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 5	RIL5-1	UID1-4	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 6	RIL6-1	UID1-5	0 or +3.3 V	FREE Board ID
9	FREE ID, Bit 7	RIL7-1	UID1-6	0 or +3.3 V	FREE Board ID
8	Mux Hold, Ch. 00	JH0	GAFE00-31		Analog held signal, GAFE Channel 0
8	Mux Shaper, Ch. 00	JSA0	GAFE00-33		Analog shaping amplifier signal, GAFE Channel 0

8	Analog VCC	TPVCC1			Analog +3.3V
8	GAFE HOLD	JHLD0	RT3-1		Hold command from GARC
10	PWR_ON_RST	TPR1	UR1-2	0V after power up	Power on Reset
12	PMT Input, Ch 00	TP151	J00		PMT Input
12	PMT Input, Ch 01	TP	J01		PMT Input
12	PMT Input, Ch 02	TP	J02		PMT Input
12	PMT Input, Ch 03	TP	J03		PMT Input
12	PMT Input, Ch 04	TP	J04		PMT Input
12	PMT Input, Ch 05	TP	J05		PMT Input
12	PMT Input, Ch 06	TP	J06		PMT Input
12	PMT Input, Ch 07	TP	J07		PMT Input
12	PMT Input, Ch 08	TP	J08		PMT Input
12	PMT Input, Ch 09	TP	J09		PMT Input
12	PMT Input, Ch 10	TP	J10		PMT Input
12	PMT Input, Ch 11	TP	J11		PMT Input
12	PMT Input, Ch 12	TP	J12		PMT Input
12	PMT Input, Ch 13	TP	J13		PMT Input
12	PMT Input, Ch 14	TP	J14		PMT Input
12	PMT Input, Ch 15	TP	J15		PMT Input
12	PMT Input, Ch 16	TP	J16		PMT Input
12	PMT Input, Ch 17	TP	J17		PMT Input
12	ADC VREF, Ch. 00	CA4-1	UADC00-5		ADC Voltage Reference
12	GAFE VREF, Ch. 00	C266-1	GAFE00-8		GAFE Internal Voltage Reference
12	GAFE VDD, Ch. 00	CA6-1	CA5-1		GAFE Digital Power
12	GAFE VCC, Ch. 00	CA7-1	CA8-1		GAFE Analog Power

Appendix 3: GARC Configuration Command Format

The GARC logic core responds only to properly structured commands. There are two possible command types – Trigger Commands and Configuration Commands. Trigger commands initiate an Event Data cycle, causing a GAFE Hold, an analog-to-digital conversion, and the return of an event data packet. Configuration commands are used to either read or write GARC or GAFE registers.

The format for Trigger Commands is detailed in the table below.

Bit(s)	Bit Description	Value
3	Start Bit	1
2:1	Trigger Type Bits	10 for ZS Enabled Trigger 01 for Send All PHA Trigger
0	Parity Bit	Odd parity bit over previous two bits

Therefore, a 1100 is a ZS Enabled Trigger command and a 1010 is a Send All PHA Trigger command.

This format for GARC Configuration Commands is detailed in the table below.

Field	# bits	Function
Start	1	1 for start
CMD Type	2	00 for command
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)
GAFE/GARC Select	1	0 for GARC 1 for GAFE
GAFE/GARC Address	5	GAFE: Select which GAFE, 0x1F for all GAFE GARC: Select which function block
Read/Write	1	0 for write, 1 for read
Data/Dataless	1	0 for dataless, 1 for data, always 1 for ACD
register/function number	4	Which register/function in the function block
CMD Parity	1	Odd parity bit over previous 15 bits
Data	16	Data Field
Data Parity	1	Odd parity bit over previous 16 bits

Appendix 4: GARC Event Data Format

The GARC core returns an event data packet when a valid trigger command is received. The event data format is detailed in the table below.

Field	# bits	Function
Start Bit	1	1 for start
Hit Map Bits	18	Bits 17-0 for channels 0-17, bit set if hit in channel
Zero Suppression Bits	18	Bits 17-0 for channels 0-17, bit set if PHA above threshold
CMD/Data ERROR	1	Error in command parity detected
Header Parity	1	Odd parity bit over previous 37 bits
PHA Words (quantity 0-18) Order: Channel 0 to channel 17	15	Bit 14: 1 if another PHA word follows this one, 0 if this is last one Bit 13: 1 for high range, 0 for low range Bits 12-1: the PHA value, 0 to 4095 Bit 0: Odd parity over last 14 bits

Appendix 5: GARC Configuration Data Readback Format

The GARC core returns an register configuration data packet when a valid configuration readback command is received. The configuration readback data format is detailed in the table below.

Field	# bits	Function
Start	1	1 for start
GAFE/GARC Select	1	Copy of write command field (0 for GARC, 1 for GAFE)
GAFE/GARC Address	5	Copy of write command field (Select which GAFE)
Read/Write	1	1 for read
Data/Dataless	1	always 1
Register/function number	4	Copy of write command field (which register/function in the function block)
CMD Parity	1	Odd parity bit over previous 12 bits
Data	16	Data, MSB first
CMD/DATA ERROR	1	Error in parity detected
Parity	1	Odd parity bit over previous 17 bits

Appendix 6: MDM Connector Pin List

Connector JHV1 to High Voltage Bias Supply #1

Connector Pin	Signal Name
JHV1 - 1	HVBS +28V
JHV1 - 2	28V RTN
JHV1 - 3	HV_MON_P1
JHV1 - 4	DAC_P
JHV1 - 5	HV_ENABLE_1
JHV1 - 6	HVBS +28V
JHV1 - 7	28V RTN
JHV1 - 8	HV_MON_N1
JHV1 - 9	DAC_N

Connector JHV2 to High Voltage Bias Supply #2

Connector Pin	Signal Name
JHV2 - 1	HVBS +28V
JHV2 - 2	28V RTN
JHV2 - 3	HV_MON_P2
JHV2 - 4	DAC_P
JHV2 - 5	HV_ENABLE_2
JHV2 - 6	HVBS +28V
JHV2 - 7	28V RTN
JHV2 - 8	HV_MON_N2
JHV2 - 9	DAC_N

Appendix 7: Series II Circular Connector Pin List

Pin Locations for Connectors JP1 and (JS2)

Signal Name	Function	Connector Pin
ACD_VDD_0A(B)	+3.3V Power to ACD	1
ACD_VDD_1A(B)	+3.3V Power to ACD	3
ACD_VDD_2A(B)	+3.3V Power to ACD	4
ACD_28V_0A(B)	+28V Power to ACD HVBS	5
ACD_28V_1A(B)	+28V Power to ACD HVBS	7
ACD_NVETO_16A(B)P	Veto Ch 16 + to AEM	17
ACD_NVETO_16A(B)M	Veto Ch 16 - to AEM	18
ACD_NVETO_17A(B)P	Veto Ch 17 + to AEM	19
ACD_NVETO_17A(B)M	Veto Ch 17 - to AEM	20
ACD_NCNO_A(B)P	CNO + to AEM	21
ACD_NCNO_A(B)M	CNO - to AEM	22
ACD_HV_AP	High Voltage Supply 1 Monitor + to AEM	23

ACD_HV_AM	High Voltage Supply 1 Monitor - to AEM	24
ACD_TEMP_A(B)P	Temp Monitor + to AEM	25
ACD_TEMP_A(B)M	Temp Monitor - to AEM	26
ACD_HV_BP	High Voltage Supply 2 Monitor + to AEM	27
ACD_HV_BM	High Voltage Supply 2 Monitor - to AEM	28
ACD_GND_0A(B)	+3.3V Power Return	30
ACD_GND_1A(B)	+3.3V Power Return	31
ACD_GND_2A(B)	+3.3V Power Return	32
ACD_28V_RTN_0A(B)	+28V Return	33
ACD_28V_RTN_1A(B)	+28V Return	34
ACD_NVETO_15A(B)M	Veto Ch 15 - to AEM	40
ACD_NVETO_15A(B)P	Veto Ch 15 + to AEM	41
ACD_NVETO_14A(B)M	Veto Ch 14 - to AEM	42
ACD_NVETO_14A(B)P	Veto Ch 14 + to AEM	43
ACD_NVETO_13A(B)M	Veto Ch 13 - to AEM	44
ACD_NVETO_13A(B)P	Veto Ch 13 + to AEM	45
ACD_NVETO_12A(B)M	Veto Ch 12 - to AEM	46
ACD_NVETO_12A(B)P	Veto Ch 12 + to AEM	47
ACD_NVETO_11A(B)M	Veto Ch 11 - to AEM	48
ACD_NVETO_11A(B)P	Veto Ch 11 + to AEM	49
ACD_NVETO_10A(B)M	Veto Ch 10 - to AEM	50
ACD_NVETO_10A(B)P	Veto Ch 10 + to AEM	51
ACD_NVETO_09A(B)M	Veto Ch 9 - to AEM	52
ACD_NVETO_09A(B)P	Veto Ch 9 + to AEM	53
ACD_NVETO_08A(B)M	Veto Ch 8 - to AEM	54
ACD_NVETO_08A(B)P	Veto Ch 8 + to AEM	55
ACD_NVETO_07A(B)M	Veto Ch 7 - to AEM	56
ACD_NVETO_07A(B)P	Veto Ch 7 + to AEM	57
ACD_NVETO_06A(B)M	Veto Ch 6 - to AEM	58
ACD_NVETO_06A(B)P	Veto Ch 6 + to AEM	59
ACD_NVETO_05A(B)M	Veto Ch 5 - to AEM	60
ACD_NVETO_05A(B)P	Veto Ch 5 + to AEM	61
ACD_NVETO_04A(B)M	Veto Ch 4 - to AEM	62
ACD_NVETO_04A(B)P	Veto Ch 4 + to AEM	63
ACD_NVETO_03A(B)M	Veto Ch 3 - to AEM	64
ACD_NVETO_03A(B)P	Veto Ch 3 + to AEM	65
ACD_NVETO_02A(B)M	Veto Ch 2 - to AEM	66
ACD_NVETO_02A(B)P	Veto Ch 2 + to AEM	67
ACD_NVETO_01A(B)M	Veto Ch 1 - to AEM	68
ACD_NVETO_01A(B)P	Veto Ch 1 + to AEM	69
ACD_NVETO_00A(B)M	Veto Ch 0 - to AEM	70
ACD_NVETO_00A(B)P	Veto Ch 0 + to AEM	71
ACD_NSDATA_A(B)M	Data- to AEM	72
ACD_NSDATA_A(B)P	Data+ to AEM	73

ACD_NRST_A(B)M	Reset- to ACD	74
ACD_NRST_A(B)P	Reset+ to ACD	75
ACD_NSCMD_A(B)M	Command- to ACD	76
ACD_NSCMD_A(B)P	Command+ to ACD	77
ACD_CLK_A(B)M	Clock- to ACD	78
ACD_CLK_A(B)P	Clock+ to ACD	79
Spare Pins	Pins 8-16, 29, 35-39 not used	rest

Appendix 8: GARC Pin List

Tanner IO Cell	MOSIS Bond Pad Name	GARC Package Pin Number	GARC Signal Name
PADGnd	L1	1	DGND
PADAREF	L2	2	ACD_CLK_AP
PADAREF	L3	3	ACD_CLK_AM
PADAREF	L4	4	ACD_CLK_BP
PADAREF	L5	5	ACD_CLK_BM
PADAREF	L6	6	ACD_NSCMD_AP
PADAREF	L7	7	ACD_NSCMD_AM
PADAREF	K8	8	ACD_NSCMD_BP
PADAREF	L9	9	ACD_NSCMD_BM
PADAREF	L10	10	ACD_NRST_AP
PADAREF	L11	11	ACD_NRST_AM
PADAREF	L12	12	ACD_NRST_BP
PADAREF	L13	13	ACD_NRST_BM
PADAREF	L14	14	ACD_NSDATA_AP
PADAREF	L15	15	ACD_NSDATA_AM
PADAREF	L16	16	ACD_NSDATA_BP
PADAREF	L17	17	ACD_NSDATA_BM
PADAREF	L18	18	ACD_NCNO_AP
PADAREF	L19	19	ACD_NCNO_AM
PADAREF	L20	20	ACD_NCNO_BP
PADAREF	L21	21	ACD_NCNO_BM
PADAREF	L22	22	ACD_NVETO_00AP
PADAREF	L23	23	ACD_NVETO_00AM
PADVdd	L24	24	DVDD
PADAREF	L25	25	ACD_NVETO_00BP
PADAREF	L26	26	ACD_NVETO_00BM
PADGnd	L27	27	DGND
PADAREF	L28	28	ACD_NVETO_01AP
PADAREF	L29	29	ACD_NVETO_01AM
PADAREF	L30	30	ACD_NVETO_01BP
PADAREF	L31	31	ACD_NVETO_01BM
PADAREF	L32	32	ACD_NVETO_02AP
PADAREF	L33	33	ACD_NVETO_02AM
PADAREF	L34	34	ACD_NVETO_02BP
PADAREF	L35	35	ACD_NVETO_02BM
PADAREF	L36	36	ACD_NVETO_03AP
PADAREF	L37	37	ACD_NVETO_03AM
PADAREF	L38	38	ACD_NVETO_03BP
PADAREF	L39	39	ACD_NVETO_03BM
PADAREF	L40	40	ACD_NVETO_04AP
PADAREF	L41	41	ACD_NVETO_04AM
PADAREF	L42	42	ACD_NVETO_04BP

PADAREF	L43	43	ACD_NVETO_04BM
PADAREF	L44	44	ACD_NVETO_05AP
PADAREF	L45	45	ACD_NVETO_05AM
PADAREF	L46	46	ACD_NVETO_05BP
PADAREF	L47	47	ACD_NVETO_05BM
PADAREF	L48	48	ACD_NVETO_06AP
PADAREF	L49	49	ACD_NVETO_06AM
PADAREF	L50	50	ACD_NVETO_06BP
PADAREF	L51	51	ACD_NVETO_06BM
PADVdd	L52	52	DVDD
PADGnd	B1	53	DGND
PADAREF	B2	54	ACD_NVETO_07AP
PADAREF	B3	55	ACD_NVETO_07AM
PADAREF	B4	56	ACD_NVETO_07BP
PADAREF	B5	57	ACD_NVETO_07BM
PADAREF	B6	58	ACD_NVETO_08AP
PADAREF	B7	59	ACD_NVETO_08AM
PADAREF	B8	60	ACD_NVETO_08BP
PADAREF	B9	61	ACD_NVETO_08BM
PADAREF	B10	62	ACD_NVETO_09AP
PADAREF	B11	63	ACD_NVETO_09AM
PADAREF	B12	64	ACD_NVETO_09BP
PADAREF	B13	65	ACD_NVETO_09BM
PADAREF	B14	66	ACD_NVETO_10AP
PADAREF	B15	67	ACD_NVETO_10AM
PADAREF	B16	68	ACD_NVETO_10BP
PADAREF	B17	69	ACD_NVETO_10BM
PADAREF	B18	70	ACD_NVETO_11AP
PADAREF	B19	71	ACD_NVETO_11AM
PADAREF	B20	72	ACD_NVETO_11BP
PADAREF	B21	73	ACD_NVETO_11BM
PADAREF	B22	74	ACD_NVETO_12AP
PADAREF	B23	75	ACD_NVETO_12AM
PADAREF	B24	76	ACD_NVETO_12BP
PADAREF	B25	77	ACD_NVETO_12BM
PADVdd	B26	78	DVDD
PADAREF	B27	79	CHID_17
PADGnd	B28	80	DGND
PADAREF	B29	81	DISC_17
PADAREF	B30	82	IRTN_17
PADAREF	B31	83	CHID_16
PADAREF	B32	84	DISC_16
PADAREF	B33	85	IRTN_16
PADAREF	B34	86	CHID_15
PADAREF	B35	87	DISC_15
PADAREF	B36	88	IRTN_15
PADAREF	B37	89	CHID_14
PADAREF	B38	90	DISC_14
PADAREF	B39	91	IRTN_14
PADAREF	B40	92	CHID_13
PADAREF	B41	93	DISC_13
PADAREF	B42	94	IRTN_13
PADAREF	B43	95	CHID_12
PADAREF	B44	96	DISC_12
PADAREF	B45	97	IRTN_12
PADAREF	B46	98	CHID_11
PADAREF	B47	99	DISC_11
PADAREF	B48	100	IRTN_11
PADAREF	B49	101	CHID_10
PADAREF	B50	102	DISC_10
PADAREF	B51	103	IRTN_10
PADAREF	B52	104	HLD_WOR_BIAS

PADAREF	R52	105	CHID_09
PADAREF	R51	106	DISC_09
PADAREF	R50	107	IRTN_09
PADAREF	R49	108	CHID_08
PADAREF	R48	109	DISC_08
PADAREF	R47	110	IRTN_08
PADAREF	R46	111	CHID_07
PADAREF	R45	112	DISC_07
PADAREF	R44	113	IRTN_07
PADAREF	R43	114	CHID_06
PADAREF	R42	115	DISC_06
PADAREF	R41	116	IRTN_06
PADAREF	R40	117	CHID_05
PADAREF	R39	118	DISC_05
PADAREF	R38	119	IRTN_05
PADAREF	R37	120	CHID_04
PADAREF	R36	121	DISC_04
PADAREF	R35	122	IRTN_04
PADAREF	R34	123	CHID_03
PADAREF	R33	124	DISC_03
PADAREF	R32	125	IRTN_03
PADAREF	R31	126	CHID_02
PADAREF	R30	127	DISC_02
PADAREF	R29	128	IRTN_02
PADAREF	R28	129	CHID_01
PADAREF	R27	130	DISC_01
PADAREF	R26	131	IRTN_01
PADVdd	R25	132	DVDD
PADAREF	R24	133	CHID_00
PADAREF	R23	134	DISC_00
PADAREF	R22	135	IRTN_00
PADGnd	R21	136	DGND
PADI _C	R20	137	PHAD_17
PADI _C	R19	138	PHAD_16
PADI _C	R18	139	PHAD_15
PADI _C	R17	140	PHAD_14
PADI _C	R16	141	PHAD_13
PADI _C	R15	142	PHAD_12
PADI _C	R14	143	PHAD_11
PADI _C	R13	144	PHAD_10
PADI _C	R12	145	PHAD_09
PADI _C	R11	146	PHAD_08
PADI _C	R10	147	PHAD_07
PADI _C	R9	148	PHAD_06
PADI _C	R8	149	PHAD_05
PADI _C	R7	150	PHAD_04
PADI _C	R6	151	PHAD_03
PADI _C	R5	152	PHAD_02
PADI _C	R4	153	PHAD_01
PADI _C	R3	154	PHAD_00
PADVdd	R2	155	DVDD
PADAREF	R1	156	BIAS_RCVR
PADGnd	T52	157	DGND
PADAREF	T51	158	IRTN HL DISC
PADAREF	T50	159	OR HL DISC
PADAREF	T49	160	BIAS DRV_H
PADAREF	T48	161	GAFE HOLD _P
PADAREF	T47	162	GAFE HOLD _M
PADAREF	T46	163	GAFE STROBEP
PADAREF	T45	164	GAFE STROBEM
PADAREF	T44	165	GAFE DATP
PADAREF	T43	166	GAFE DATM

PADAREF	T42	167	GAFE_CLKP
PADAREF	T41	168	GAFE_CLKM
PADAREF	T40	169	BIAS_DRV_L
PADIc	T39	170	GAFE_RET_DATA
PadOut	T38	171	GAFE_RST
PADOut	T37	172	ADC_CLK
PADOut	T36	173	NADC_CS
PADOut	T35	174	DAC_CLK
PADOut	T34	175	DAC_DATA
PADIc	T33	176	DAC_READBACK
PADOut	T32	177	NDAC_CS
PADOut	T31	178	NDAC_CLR
PADOut	T30	179	HITMAP_TEST
PADOut	T29	180	TRIG_TST
PADIc	T28	181	FREE_ID
PADIc	T27	182	PWR_ON_RST
PADOut	T26	183	VETO_ENA_TST
PADAREF	T25	184	LVDS_PRESETADJ
PADOut	T24	185	HV_ENABLE_1
PADOut	T23	186	HV_ENABLE_2
PADGnd	T22	187	DGND
PADAREF	T21	188	ACD_NVETO_17AP
PADAREF	T20	189	ACD_NVETO_17AM
PADAREF	T19	190	ACD_NVETO_17BP
PADAREF	T18	191	ACD_NVETO_17BM
PADAREF	T17	192	ACD_NVETO_16AP
PADAREF	T16	193	ACD_NVETO_16AM
PADAREF	T15	194	ACD_NVETO_16BP
PADAREF	T14	195	ACD_NVETO_16BM
PADAREF	T13	196	ACD_NVETO_15AP
PADAREF	T12	197	ACD_NVETO_15AM
PADAREF	T11	198	ACD_NVETO_15BP
PADAREF	T10	199	ACD_NVETO_15BM
PADAREF	T9	200	ACD_NVETO_14AP
PADAREF	T8	201	ACD_NVETO_14AM
PADAREF	T7	202	ACD_NVETO_14BP
PADAREF	T6	203	ACD_NVETO_14BM
PADAREF	T5	204	ACD_NVETO_13AP
PADAREF	T4	205	ACD_NVETO_13AM
PADAREF	T3	206	ACD_NVETO_13BP
PADAREF	T2	207	ACD_NVETO_13BM
PADVdd	T1	208	DVDD

Appendix 9: GAFE Pin List

Tanner IO Cell	MOSIS Bond Pad Name	GAFE Package Pin Number	GAFE Signal Name
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD
PADTBD	L1	1	TBD

Appendix 10: GARC Command Mnemonics and Functions

The following table represents each of the available GARC commands. Additionally, all GAFE commands are passed through the GARC. These command patterns are detailed in the document discussing the GAFE logic. There are two types of GARC commands – trigger commands (4 bits in length) and configuration commands (34 bits in length). The AEM-ACD ICD contains the authoritative formats for all command types, but they are repeated in the appendices of this document for convenience. The table below defines the command mnemonics that will be used in this test.

Note that a GAFE will process a write command either for the address hard-wired to the chip address pins or to an address of ‘h1F, the GAFE broadcast address. A GAFE will process a read command only for an address identical to the hard-wired address. It is an operational constraint that, for any given ACD circuit board, each GAFE must have a unique address.

GARC Cmd No.	ACD Command Mnemonic	Rd/Wr Status	Select GARC=0 GAFE=1	Function Block	Register Number	No. of Data Bits	Command Function
1	Trigger_ZS	N/A	N/A	N/A	N/A	N/A	ACD Trigger, Zero-Suppression Enable
2	Trigger_NOZS	N/A	N/A	N/A	N/A	N/A	ACD Trigger, No Zero-Suppression
3	GARC_Reset	W	0	0	1	0	Generates reset for GARC and GAFE registers
4	Veto_Delay_Wr	W	0	0	2	5	Sets Delay from Disc_In to VETO Out
5	Veto_Delay_Rd	R	0	0	2	5	Reads contents of Veto_Delay register
6	GARC_Cal_Strobe	W	0	0	3	0	Sends Calibration Strobe signal to all GAFEs
7	HVBS_Level_Wr	W	0	0	8	12	Sets GARC register value from which HVBS may be commanded in the science mode
8	HVBS_Level_Rd	R	0	0	8	12	Reads contents of HVBS Level register
9	SAA_Level_Wr	W	0	0	9	12	Sets GARC register value from which HVBS may be commanded when in the SAA
10	SAA_Level_Rd	R	0	0	9	12	Reads contents of SAA Level register
11	Use_HV_Normal	W	0	0	10	0	Sends 12 bit value in HVBS Level register to the MAX5121 DAC
12	DAC_HVReg_Rd	R	0	0	10	0	Reads MAX5121 DAC Config Register
13	Use_SAA_Normal	W	0	0	11	0	Sends 12 bit value in SAA Level register to the MAX5121 DAC
14	DAC_SAAReg_Rd	R	0	0	11	0	Reads MAX5121 DAC Config Register
15	Hold_Delay_Wr	W	0	0	12	7	Sets GARC Hold Delay
16	Hold_Delay_Rd	R	0	0	12	7	Reads back value of GARC Hold Delay register
17	Veto_Width_Wr	W	0	0	13	3	Sets width of the VETO signals
18	Veto_Width_Rd	R	0	0	13	3	Reads back width of the VETO width register
19	HitMap_Width_Wr	W	0	0	14	4	Sets width of HitMap pulses
20	HitMap_Width_Rd	R	0	0	14	4	Reads back value in the HitMap width register
21	HitMap_Deadtime_Wr	W	0	0	15	3	Sets stretch at end of HitMap pulses
22	HitMap_Deadtime_Rd	R	0	0	15	3	Sets stretch at end of HitMap pulses
23	Look_At_Me	W	0	1	4	16	GARC interface selection command (primary/secondary)
24	HitMap_Delay_Wr	W	0	1	8	5	Sets delay from Disc_In to HitMap pulse
25	HitMap_Delay_Rd	R	0	1	8	5	Reads back contents of the HitMap_Delay register
26	PHA_EN0_Wr	W	0	1	9	16	Enables and Disables PHA readout enable, channels 0 -15

27	PHA_EN0_Rd	R	0	1	9	16	Reads back contents of the PHA_EN0 register
28	VETO_EN0_Wr	W	0	1	10	16	Enables and Disables VETO signals, channels 0 -15
29	VETO_EN0_Rd	R	0	1	10	16	Reads back contents of the VETO_EN0 register
30	PHA_EN1_Wr	W	0	1	12	2	Enables and Disables PHA readout enable, channels 16 & 17
31	PHA_EN1_Rd	R	0	1	12	2	Reads back contents of the PHA_EN1 register
32	VETO_EN1_Wr	W	0	1	13	2	Enables and Disables VETO signals, channels 16 & 17
33	VETO_EN1_Rd	R	0	1	13	2	Reads back contents of the VETP_EN1 register
34	Max_PHA_Wr	W	0	1	15	5	Sets the Maximum number (limit) of PHA to be returned in a single event data packet
35	Max_PHA_Rd	R	0	1	15	5	Reads back the contents of the Max_PHA register
36	GARC_Mode_Wr	W	0	2	8	11	Sets values of GARC mode bits
37	GARC_Mode_Rd	R	0	2	8	11	Reads back the value of the GARC mode register
38	GARC_Status	R	0	2	9	6	Reads back the value of the GARC status register
39	GARC_Cmd_Reg	R	0	2	10	16	Reads back the value of the GARC command register
40	GARC_Diagnostic	R	0	2	11	16	Reads back the value of the GARC diagnostic register
41	GARC_Cmd_Rejects	R	0	2	12	8	Reads back the number of rejected commands since reset
42	FREE_Board_ID	R	0	2	13	8	Reads back the FREE board serial number
43	GARC_Version	R	0	2	14	3	Reads back the GARC ASIC version number
44	PHA_Thresh00_Wr	W	0	3	8	12	Writes PHA ZS threshold for channel 00
45	PHA_Thresh00_Rd	R	0	3	8	12	Reads back PHA ZS threshold register for channel 00
46	PHA_Thresh01_Wr	W	0	3	9	12	Writes PHA ZS threshold for channel 01
47	PHA_Thresh01_Rd	R	0	3	9	12	Reads back PHA ZS threshold register for channel 01
48	PHA_Thresh02_Wr	W	0	3	10	12	Writes PHA ZS threshold for channel 02
49	PHA_Thresh02_Rd	R	0	3	10	12	Reads back PHA ZS threshold register for channel 02
50	PHA_Thresh03_Wr	W	0	3	11	12	Writes PHA ZS threshold for channel 03
51	PHA_Thresh03_Rd	R	0	3	11	12	Reads back PHA ZS threshold register for channel 03
52	PHA_Thresh04_Wr	W	0	3	12	12	Writes PHA ZS threshold for channel 04
53	PHA_Thresh04_Rd	R	0	3	12	12	Reads back PHA ZS threshold register for channel 04
54	PHA_Thresh05_Wr	W	0	3	13	12	Writes PHA ZS threshold for channel 05
55	PHA_Thresh05_Rd	R	0	3	13	12	Reads back PHA ZS threshold register for channel 05
56	PHA_Thresh06_Wr	W	0	3	14	12	Writes PHA ZS threshold for channel 06
57	PHA_Thresh06_Rd	R	0	3	14	12	Reads back PHA ZS threshold register for channel 06
58	PHA_Thresh07_Wr	W	0	4	8	12	Writes PHA ZS threshold for channel 07
59	PHA_Thresh07_Rd	R	0	4	8	12	Reads back PHA ZS threshold register for channel 07
60	PHA_Thresh08_Wr	W	0	4	9	12	Writes PHA ZS threshold for channel 08
61	PHA_Thresh08_Rd	R	0	4	9	12	Reads back PHA ZS threshold register for channel 08
62	PHA_Thresh09_Wr	W	0	4	10	12	Writes PHA ZS threshold for channel 09
63	PHA_Thresh09_Rd	R	0	4	10	12	Reads back PHA ZS threshold register

						for channel 09	
64	PHA_Thresh10_Wr	W	0	4	11	12	Writes PHA ZS threshold for channel 10
65	PHA_Thresh10_Rd	R	0	4	11	12	Reads back PHA ZS threshold register for channel 10
66	PHA_Thresh11_Wr	W	0	4	12	12	Writes PHA ZS threshold for channel 11
67	PHA_Thresh11_Rd	R	0	4	12	12	Reads back PHA ZS threshold register for channel 11
68	PHA_Thresh12_Wr	W	0	4	13	12	Writes PHA ZS threshold for channel 12
69	PHA_Thresh12_Rd	R	0	4	13	12	Reads back PHA ZS threshold register for channel 12
70	PHA_Thresh13_Wr	W	0	4	14	12	Writes PHA ZS threshold for channel 13
71	PHA_Thresh13_Rd	R	0	4	14	12	Reads back PHA ZS threshold register for channel 13
72	PHA_Thresh14_Wr	W	0	5	8	12	Writes PHA ZS threshold for channel 14
73	PHA_Thresh14_Rd	R	0	5	8	12	Reads back PHA ZS threshold register for channel 14
74	PHA_Thresh15_Wr	W	0	5	9	12	Writes PHA ZS threshold for channel 15
75	PHA_Thresh15_Rd	R	0	5	9	12	Reads back PHA ZS threshold register for channel 15
76	PHA_Thresh16_Wr	W	0	5	10	12	Writes PHA ZS threshold for channel 16
77	PHA_Thresh16_Rd	R	0	5	10	12	Reads back PHA ZS threshold register for channel 16
78	PHA_Thresh17_Wr	W	0	5	11	12	Writes PHA ZS threshold for channel 17
79	PHA_Thresh17_Rd	R	0	5	11	12	Reads back PHA ZS threshold register for channel 17
80	ADC_TACQ_Wr	W	0	5	12	6	Sets ADC Acquisition Time from Hold to Start of Conversion
81	ADC_TACQ_Rd	R	0	5	12	6	Reads back contents of the ADC_TACQ register
82	GAFE_Mode_Wr	W	1	GAFE Addr	0	16	Writes the GAFE mode register for the ASIC addressed
83	GAFE_Mode_Rd	R	1	GAFE Addr	0	16	Reads the GAFE mode register contents for the ASIC addressed
84	GAFE_VETO_Wr	W	1	GAFE Addr	1	6	Writes the DAC1 register in the GAFE addressed
85	GAFE_VETO_Rd	R	1	GAFE Addr	1	6	Reads back the contents of the DAC1 register in the addressed GAFE
86	GAFE_VERNIER_Wr	W	1	GAFE Addr	2	6	Writes the DAC2 register in the GAFE addressed
87	GAFE_VERNIER_Rd	R	1	GAFE Addr	2	6	Reads back the contents of the DAC2 register in the addressed GAFE
88	GAFE_HLD_Wr	W	1	GAFE Addr	3	6	Writes the DAC3 register in the GAFE addressed
89	GAFE_HLD_Rd	R	1	GAFE Addr	3	6	Reads back the contents of the DAC3 register in the addressed GAFE
90	GAFE_BIAS_Wr	W	1	GAFE Addr	4	6	Writes the DAC4 register in the GAFE addressed
91	GAFE_BIAS_Rd	R	1	GAFE Addr	4	6	Reads back the contents of the DAC4 register in the addressed GAFE
92	GAFE_TCI_Wr	W	1	GAFE Addr	5	6	Writes the DAC5 register in the GAFE addressed
93	GAFE_TCI_Rd	R	1	GAFE Addr	5	6	Reads back the contents of the DAC5 register in the addressed GAFE
94	GAFE_Version	R	1	GAFE Addr	6	3	Reads back the GAFE ASIC version
95	GAFE_Write_Ctr	R	1	GAFE Addr	7	8	Reads back the contents of the GAFE write counter register
96	GAFE_Reject_Ctr	R	1	GAFE Addr	8	8	Reads back the contents of the GAFE command reject register
97	GAFE_Cmd_Ctr	R	1	GAFE Addr	9	8	Reads back the contents of the GAFE command counter
98	GAFE_Chip_Addr	R	1	GAFE Addr	10	5	Reads back the hardwired address of a GAFE ASIC

Appendix 11: Test Results Record

All measurements and test results will be recorded in this Test Results Record. A copy of the entire this entire document is not required each time the test is performed. The appendix will serve as the official record each time this test is performed.

4.0 QA Signoff

Quality Assurance approval to proceed with the test - _____
(NOTE: If QA gives verbal approval to proceed but is not in attendance for the test, record the date and the time of approval.)

4.1 FREE Assembly Identification

The test conductor for this test is: _____

Date the test started: _____

The serial number of the FREE card assembly is: _____

The identification/Serial Number listed on the GARC ASIC is: _____

The identification/Serial Numbers listed on the GAFE ASICs are:

GAFE Channel	ASIC Serial Number
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

4.2 Test Equipment Utilized

Instrument Type	Manufacturer & Model Number	NASA ID Number	Calibration Due Date
Power Supply for HVBS +28V			
Power Supply for FREE & GSE +3.3V & +5.0V			
Multimeter 1			
Multimeter 2			
Test Pulse Generator			
Oscilloscope			
AC Current Probe			
RMS Voltmeter			
Pulse Generator			
Charge Terminator Box			

5.1 Electrical Continuity Check

Test Omitted - _____

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_VDD	JP1 - 3	JP1 - 1	R < 1 Ω	
2	ACD_VDD	JP1 - 4	JP1 - 1	R < 1 Ω	
3	ACD_VDD	JS2 - 1	JP1 - 1	R < 1 Ω	
4	ACD_VDD	JS2 - 3	JP1 - 1	R < 1 Ω	
5	ACD_VDD	JS2 - 4	JP1 - 1	R < 1 Ω	
6	ACD_RTN	JP1-31	JP1-30	R < 1 Ω	
7	ACD_RTN	JP1-32	JP1-30	R < 1 Ω	
8	ACD_RTN	JS2-30	JP1-30	R < 1 Ω	
9	ACD_RTN	JS2-31	JP1-30	R < 1 Ω	
10	ACD_RTN	JS2-32	JP1-30	R < 1 Ω	
11	ACD_28V	JP1-7	JP1-5	R < 1 Ω	
12	ACD_28V	JS2-5	JP1-5	R < 1 Ω	

13	ACD_28V	JS2-7	JP1-5	R < 1 Ω	
14	ACD_28V	JHV1-1	JP1-5	R < 1 Ω	
15	ACD_28V	JHV1-6	JP1-5	R < 1 Ω	
16	ACD_28V	JHV2-1	JP1-5	R < 1 Ω	
17	ACD_28V	JHV2-6	JP1-5	R < 1 Ω	
18	ACD_28V_RTN	JP1-34	JP1-33	R < 1 Ω	
19	ACD_28V_RTN	JS2-33	JP1-33	R < 1 Ω	
20	ACD_28V_RTN	JS2-34	JP1-33	R < 1 Ω	
21	ACD_28V_RTN	JHV1-2	JP1-33	R < 1 Ω	
22	ACD_28V_RTN	JHV1-7	JP1-33	R < 1 Ω	
23	ACD_28V_RTN	JHV2-2	JP1-33	R < 1 Ω	
24	ACD_28V_RTN	JHV2-7	JP1-33	R < 1 Ω	
25	HV_DACP	JHV1-4	JHV2-4	R < 1 Ω	
26	HV_DACN	JHV1-9	JHV2-9	R < 1 Ω	
27	HV1_MONP	JHV1-3	JP1-23	R < 1 Ω	
28	HV1_MONP	JHV1-3	JS2-23	R < 1 Ω	
29	HV1_MONN	JHV1-8	JP1-24	R < 1 Ω	
30	HV1_MONN	JHV1-8	JS2-24	R < 1 Ω	
31	HV2_MONP	JHV2-3	JP1-27	R < 1 Ω	
32	HV2_MONP	JHV2-3	JS2-27	R < 1 Ω	
33	HV2_MONN	JHV2-8	JP1-28	R < 1 Ω	
34	HV2_MONN	JHV2-8	JS2-28	R < 1 Ω	

5.2 Electrical Isolation Check

Test Omitted - _____

Meas. No.	Signal 1	Signal 2	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_VDD	ACD_RTN	JP1 - 1	JP1 - 30	R > 1 kΩ	
2	ACD_VDD	ACD_28V	JP1 - 1	JP1 - 5	R > 1 MΩ	
3	ACD_VDD	ACD_28V_RTN	JP1 - 1	JP1 - 33	R > 1 MΩ	
4	ACD_28V	ACD_RTN	JP1 - 5	JP1 - 30	R > 1 MΩ	
5	ACD_28V	ACD_28V_RTN	JP1 - 5	JP1 - 33	R > 1 kΩ	
6	ACD_RTN	ACD_28V_RTN	JS2 - 30	JP1 - 33	R > 90 Ω	
7	ACD_NVETO_00AP	ACD_NVETO_00AM	JP1-70	JP1-71	R > 40 kΩ	
8	ACD_NVETO_01AP	ACD_NVETO_01AM	JP1-68	JP1-69	R > 40 kΩ	
9	ACD_NVETO_02AP	ACD_NVETO_02AM	JP1-66	JP1-67	R > 40 kΩ	
10	ACD_NVETO_03AP	ACD_NVETO_03AM	JP1-64	JP1-65	R > 40 kΩ	
11	ACD_NVETO_04AP	ACD_NVETO_04AM	JP1-62	JP1-63	R > 40 kΩ	
12	ACD_NVETO_05AP	ACD_NVETO_05AM	JP1-60	JP1-61	R > 40 kΩ	
13	ACD_NVETO_06AP	ACD_NVETO_06AM	JP1-58	JP1-59	R > 40 kΩ	
14	ACD_NVETO_07AP	ACD_NVETO_07AM	JP1-56	JP1-57	R > 40 kΩ	
15	ACD_NVETO_08AP	ACD_NVETO_08AM	JP1-54	JP1-55	R > 40 kΩ	
16	ACD_NVETO_09AP	ACD_NVETO_09AM	JP1-52	JP1-53	R > 40 kΩ	
17	ACD_NVETO_10AP	ACD_NVETO_10AM	JP1-50	JP1-51	R > 40 kΩ	
18	ACD_NVETO_11AP	ACD_NVETO_11AM	JP1-48	JP1-49	R > 40 kΩ	
19	ACD_NVETO_12AP	ACD_NVETO_12AM	JP1-46	JP1-47	R > 40 kΩ	
20	ACD_NVETO_13AP	ACD_NVETO_13AM	JP1-44	JP1-45	R > 40 kΩ	
21	ACD_NVETO_14AP	ACD_NVETO_14AM	JP1-42	JP1-43	R > 40 kΩ	
22	ACD_NVETO_15AP	ACD_NVETO_15AM	JP1-40	JP1-41	R > 40 kΩ	
23	ACD_NVETO_16AP	ACD_NVETO_16AM	JP1-17	JP1-18	R > 40 kΩ	

24	ACD_NVETO_17AP	ACD_NVETO_17AM	JP1-19	JP1-20	R > 40 kΩ	
25	ACD_NCNO_AP	ACD_NCNO_AM	JP1-21	JP1-22	R > 40 kΩ	
26	ACD_NSDATA_AP	ACD_NSDATA_AM	JP1-72	JP1-73	R > 40 kΩ	
27	ACD_NRST_AP	ACD_NTST_AM	JP1-74	JP1-75	95 Ω < R < 105 Ω	
28	ACD_NSCMD_AP	ACD_NSCMD_AM	JP1-76	JP1-77	95 Ω < R < 105 Ω	
29	ACD_NSCLK_AP	ACD_NSCLK_AM	JP1-78	JP1-79	95 Ω < R < 105 Ω	
30	ACD_HV_AP	ACD_HV_AM	JP1-23	JP1-24	R > 100 kΩ	
31	ACD_TEMP_AP	ACD_TEMP_AM	JP1-25	JP1-26	R > 20 kΩ	
32	ACD_NVETO_00BP	ACD_NVETO_00BM	JS2-70	JS2-71	R > 40 kΩ	
33	ACD_NVETO_01BP	ACD_NVETO_01BM	JS2-68	JS2-69	R > 40 kΩ	
34	ACD_NVETO_02BP	ACD_NVETO_02BM	JS2-66	JS2-67	R > 40 kΩ	
35	ACD_NVETO_03BP	ACD_NVETO_03BM	JS2-64	JS2-65	R > 40 kΩ	
36	ACD_NVETO_04BP	ACD_NVETO_04BM	JS2-62	JS2-63	R > 40 kΩ	
37	ACD_NVETO_05BP	ACD_NVETO_05BM	JS2-60	JS2-61	R > 40 kΩ	
38	ACD_NVETO_06BP	ACD_NVETO_06BM	JS2-58	JS2-59	R > 40 kΩ	
39	ACD_NVETO_07BP	ACD_NVETO_07BM	JS2-56	JS2-57	R > 40 kΩ	
40	ACD_NVETO_08BP	ACD_NVETO_08BM	JS2-54	JS2-55	R > 40 kΩ	
41	ACD_NVETO_09BP	ACD_NVETO_09BM	JS2-52	JS2-53	R > 40 kΩ	
42	ACD_NVETO_10BP	ACD_NVETO_10BM	JS2-50	JS2-51	R > 40 kΩ	
43	ACD_NVETO_11BP	ACD_NVETO_11BM	JS2-48	JS2-49	R > 40 kΩ	
44	ACD_NVETO_12BP	ACD_NVETO_12BM	JS2-46	JS2-47	R > 40 kΩ	
45	ACD_NVETO_13BP	ACD_NVETO_13BM	JS2-44	JS2-45	R > 40 kΩ	
46	ACD_NVETO_14BP	ACD_NVETO_14BM	JS2-42	JS2-43	R > 40 kΩ	
47	ACD_NVETO_15BP	ACD_NVETO_15BM	JS2-40	JS2-41	R > 40 kΩ	
48	ACD_NVETO_16BP	ACD_NVETO_16BM	JS2-17	JS2-18	R > 40 kΩ	
49	ACD_NVETO_17BP	ACD_NVETO_17BM	JS2-19	JS2-20	R > 40 kΩ	
50	ACD_NCNO_BP	ACD_NCNO_BM	JS2-21	JS2-22	R > 40 kΩ	
51	ACD_NSDATA_BP	ACD_NSDATA_BM	JS2-72	JS2-73	R > 40 kΩ	
52	ACD_NRST_BP	ACD_NTST_BM	JS2-74	JS2-75	95 Ω < R < 105 Ω	
53	ACD_NSCMD_BP	ACD_NSCMD_BM	JS2-76	JS2-77	95 Ω < R < 105 Ω	
54	ACD_NSCLK_BP	ACD_NSCLK_BM	JS2-78	JS2-79	95 Ω < R < 105 Ω	
55	ACD_HV_BP	ACD_HV_BM	JS2-23	JS2-24	R > 100 kΩ	
56	ACD_TEMP_BP	ACD_TEMP_BM	JS2-25	JS2-26	R > 20 kΩ	

5.3 Verification of Proper LVDS Terminations

Test Omitted - _____

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_NVETO_16_A	JP1 - 17	JP1 - 18	95 Ω < R < 105 Ω	
2	ACD_NVETO_17_A	JP1 - 19	JP1 - 20	95 Ω < R < 105 Ω	
3	ACD_CNO_A	JP1 - 21	JP1 - 22	95 Ω < R < 105 Ω	
4	ACD_NVETO_15_A	JP1 - 40	JP1 - 41	95 Ω < R < 105 Ω	
5	ACD_NVETO_14_A	JP1 - 42	JP1 - 43	95 Ω < R < 105 Ω	
6	ACD_NVETO_13_A	JP1 - 44	JP1 - 45	95 Ω < R < 105 Ω	
7	ACD_NVETO_12_A	JP1 - 46	JP1 - 47	95 Ω < R < 105 Ω	
8	ACD_NVETO_11_A	JP1 - 48	JP1 - 49	95 Ω < R < 105 Ω	
9	ACD_NVETO_10_A	JP1 - 50	JP1 - 51	95 Ω < R < 105 Ω	
10	ACD_NVETO_09_A	JP1 - 52	JP1 - 53	95 Ω < R < 105 Ω	
11	ACD_NVETO_08_A	JP1 - 54	JP1 - 55	95 Ω < R < 105 Ω	
12	ACD_NVETO_07_A	JP1 - 56	JP1 - 57	95 Ω < R < 105 Ω	

13	ACD_NVETO_06_A	JP1 - 58	JP1 - 59	95 Ω < R < 105 Ω	
14	ACD_NVETO_05_A	JP1 - 60	JP1 - 61	95 Ω < R < 105 Ω	
15	ACD_NVETO_04_A	JP1 - 62	JP1 - 63	95 Ω < R < 105 Ω	
16	ACD_NVETO_03_A	JP1 - 64	JP1 - 65	95 Ω < R < 105 Ω	
17	ACD_NVETO_02_A	JP1 - 66	JP1 - 67	95 Ω < R < 105 Ω	
18	ACD_NVETO_01_A	JP1 - 68	JP1 - 69	95 Ω < R < 105 Ω	
19	ACD_NVETO_00_A	JP1 - 70	JP1 - 71	95 Ω < R < 105 Ω	
20	ACD_NSDATA_A	JP1 - 72	JP1 - 73	95 Ω < R < 105 Ω	
21	ACD_NRST_A	JP1 - 74	JP1 - 75	R > 100 kΩ	
22	ACD_NS CMD_A	JP1 - 76	JP1 - 77	R > 100 kΩ	
23	ACD_CLK_A	JP1 - 78	JP1 - 79	R > 100 kΩ	
24	ACD_NVETO_16_B	JS2 - 17	JS2 - 18	95 Ω < R < 105 Ω	
25	ACD_NVETO_17_B	JS2 - 19	JS2 - 20	95 Ω < R < 105 Ω	
26	ACD_CNO_B	JS2 - 21	JS2 - 22	95 Ω < R < 105 Ω	
27	ACD_NVETO_15_B	JS2 - 40	JS2 - 41	95 Ω < R < 105 Ω	
28	ACD_NVETO_14_B	JS2 - 42	JS2 - 43	95 Ω < R < 105 Ω	
29	ACD_NVETO_13_B	JS2 - 44	JS2 - 45	95 Ω < R < 105 Ω	
30	ACD_NVETO_12_B	JS2 - 46	JS2 - 47	95 Ω < R < 105 Ω	
31	ACD_NVETO_11_B	JS2 - 48	JS2 - 49	95 Ω < R < 105 Ω	
32	ACD_NVETO_10_B	JS2 - 50	JS2 - 51	95 Ω < R < 105 Ω	
33	ACD_NVETO_09_B	JS2 - 52	JS2 - 53	95 Ω < R < 105 Ω	
34	ACD_NVETO_08_B	JS2 - 54	JS2 - 55	95 Ω < R < 105 Ω	
35	ACD_NVETO_07_B	JS2 - 56	JS2 - 57	95 Ω < R < 105 Ω	
36	ACD_NVETO_06_B	JS2 - 58	JS2 - 59	95 Ω < R < 105 Ω	
37	ACD_NVETO_05_B	JS2 - 60	JS2 - 61	95 Ω < R < 105 Ω	
38	ACD_NVETO_04_B	JS2 - 62	JS2 - 63	95 Ω < R < 105 Ω	
39	ACD_NVETO_03_B	JS2 - 64	JS2 - 65	95 Ω < R < 105 Ω	
40	ACD_NVETO_02_B	JS2 - 66	JS2 - 67	95 Ω < R < 105 Ω	
41	ACD_NVETO_01_B	JS2 - 68	JS2 - 69	95 Ω < R < 105 Ω	
42	ACD_NVETO_00_B	JS2 - 70	JS2 - 71	95 Ω < R < 105 Ω	
43	ACD_NSDATA_B	JS2 - 72	JS2 - 73	95 Ω < R < 105 Ω	
44	ACD_NRST_B	JS2 - 74	JS2 - 75	R > 100 kΩ	
45	ACD_NS CMD_B	JS2 - 76	JS2 - 77	R > 100 kΩ	
46	ACD_CLK_B	JS2 - 78	JS2 - 79	R > 100 kΩ	

6.1 Stray Voltage Test at the AEM Interface

Test Omitted - _____

Meas. No.	AEM Interface Pin	Signal Name	Expected Voltage	Measured Voltage
1	JP1 - 1	ACD_VDD_0A	+3.3V	
2	JP1 - 3	ACD_VDD_1A	+3.3V	
3	JP1 - 4	ACD_VDD_2A	+3.3V	
4	JP1 - 5	ACD_28V_0A	+28V	
5	JP1 - 7	ACD_28V_1A	+28V	
6	JP1 - 17	ACD_NVETO_16AP	0 < V < 3.3	
7	JP1 - 18	ACD_NVETO_16AM	0 < V < 3.3	
8	JP1 - 19	ACD_NVETO_17AP	0 < V < 3.3	
9	JP1 - 20	ACD_NVETO_17AM	0 < V < 3.3	
10	JP1 - 21	ACD_NCNO_AP	0 < V < 3.3	

11	JP1 - 22	ACD_NCNO_AM	0< V < 3.3	
12	JP1 - 23	ACD_HV_AP	0< V < 3.3	
13	JP1 - 24	ACD_HV_AM	0< V < 3.3	
14	JP1 - 25	ACD_TEMP_AP	TBD	
15	JP1 - 26	ACD_TEMP_AM	TBD	
16	JP1 - 30	ACD_GND_0A	0	
17	JP1 - 31	ACD_GND_1A	0	
18	JP1 - 32	ACD_GND_2A	0	
19	JP1 - 33	ACD_28V_RTN_0A	0	
20	JP1 - 34	ACD_28V_RTN_1A	0	
21	JP1 - 40	ACD_NVETO_15AM	V < 200mV	
22	JP1 - 41	ACD_NVETO_15AP	V < 200mV	
23	JP1 - 42	ACD_NVETO_14AM	V < 200mV	
24	JP1 - 43	ACD_NVETO_14AP	V < 200mV	
25	JP1 - 44	ACD_NVETO_13AM	V < 200mV	
26	JP1 - 45	ACD_NVETO_13AP	V < 200mV	
27	JP1 - 46	ACD_NVETO_12AM	V < 200mV	
28	JP1 - 47	ACD_NVETO_12AP	V < 200mV	
29	JP1 - 48	ACD_NVETO_11AM	V < 200mV	
31	JP1 - 50	ACD_NVETO_10AM	V < 200mV	
32	JP1 - 51	ACD_NVETO_10AP	V < 200mV	
33	JP1 - 52	ACD_NVETO_09AM	V < 200mV	
34	JP1 - 53	ACD_NVETO_09AP	V < 200mV	
35	JP1 - 54	ACD_NVETO_08AM	V < 200mV	
36	JP1 - 55	ACD_NVETO_08AP	V < 200mV	
37	JP1 - 56	ACD_NVETO_07AM	V < 200mV	
38	JP1 - 57	ACD_NVETO_07AP	V < 200mV	
39	JP1 - 58	ACD_NVETO_06AM	V < 200mV	
40	JP1 - 59	ACD_NVETO_06AP	V < 200mV	
41	JP1 - 60	ACD_NVETO_05AM	V < 200mV	
42	JP1 - 61	ACD_NVETO_05AP	V < 200mV	
43	JP1 - 62	ACD_NVETO_04AM	V < 200mV	
44	JP1 - 63	ACD_NVETO_04AP	V < 200mV	
45	JP1 - 64	ACD_NVETO_03AM	V < 200mV	
46	JP1 - 65	ACD_NVETO_03AP	V < 200mV	
47	JP1 - 66	ACD_NVETO_02AM	V < 200mV	
48	JP1 - 67	ACD_NVETO_02AP	V < 200mV	
49	JP1 - 68	ACD_NVETO_01AM	V < 200mV	
50	JP1 - 69	ACD_NVETO_01AP	V < 200mV	
51	JP1 - 70	ACD_NVETO_00AM	V < 200mV	
52	JP1 - 71	ACD_NVETO_00AP	V < 200mV	
53	JP1 - 72	ACD_NS DATA_AM	V < 200mV	
54	JP1 - 73	ACD_NS DATA_AP	V < 200mV	
55	JP1 - 74	ACD_NRST_AM	V < 200mV	
56	JP1 - 75	ACD_NRST_AP	V > 2.3V	
57	JP1 - 76	ACD_NSCMD_AM	V < 200mV	
58	JP1 - 77	ACD_NSCMD_AP	V > 2.3V	
59	JP1 - 78	ACD_CLK_AM	1.1V < V < 1.5V	
60	JP1 - 79	ACD_CLK_AP	1.1V < V < 1.5V	
61	JS2 - 1	ACD_VDD_0B	+3.3V	
62	JS2 - 3	ACD_VDD_1B	+3.3V	

63	JS2 - 4	ACD_VDD_2B	+3.3V	
64	JS2 - 5	ACD_28V_0B	+28V	
65	JS2 - 7	ACD_28V_1B	+28V	
66	JS2 - 17	ACD_NVETO_16BP	V < 200mV	
67	JS2 - 18	ACD_NVETO_16BM	V < 200mV	
68	JS2 - 19	ACD_NVETO_17BP	V < 200mV	
69	JS2 - 20	ACD_NVETO_17BM	V < 200mV	
70	JS2 - 21	ACD_NCNO_BP	V < 200mV	
71	JS2 - 22	ACD_NCNO_BM	V < 200mV	
72	JS2 - 23	ACD_HV_BP	V < 200mV	
73	JS2 - 24	ACD_HV_BM	V < 200mV	
74	JS2 - 25	ACD_TEMP_BP	TBD	
75	JS2 - 26	ACD_TEMP_BM	TBD	
76	JS2 - 30	ACD_GND_0B	0	
77	JS2 - 31	ACD_GND_1B	0	
78	JS2 - 32	ACD_GND_2B	0	
79	JS2 - 33	ACD_28V_RTN_0B	0	
80	JS2 - 34	ACD_28V_RTN_1B	0	
81	JS2 - 40	ACD_NVETO_15BM	V < 200mV	
82	JS2 - 41	ACD_NVETO_15BP	V < 200mV	
83	JS2 - 42	ACD_NVETO_14BM	V < 200mV	
84	JS2 - 43	ACD_NVETO_14BP	V < 200mV	
85	JS2 - 44	ACD_NVETO_13BM	V < 200mV	
86	JS2 - 45	ACD_NVETO_13BP	V < 200mV	
87	JS2 - 46	ACD_NVETO_12BM	V < 200mV	
88	JS2 - 47	ACD_NVETO_12BP	V < 200mV	
89	JS2 - 48	ACD_NVETO_11BM	V < 200mV	
90	JS2 - 49	ACD_NVETO_11BP	V < 200mV	
91	JS2 - 50	ACD_NVETO_10BM	V < 200mV	
92	JS2 - 51	ACD_NVETO_10BP	V < 200mV	
93	JS2 - 52	ACD_NVETO_09BM	V < 200mV	
94	JS2 - 53	ACD_NVETO_09BP	V < 200mV	
95	JS2 - 54	ACD_NVETO_08BM	V < 200mV	
96	JS2 - 55	ACD_NVETO_08BP	V < 200mV	
97	JS2 - 56	ACD_NVETO_07BM	V < 200mV	
98	JS2 - 57	ACD_NVETO_07BP	V < 200mV	
99	JS2 - 58	ACD_NVETO_06BM	V < 200mV	
100	JS2 - 59	ACD_NVETO_06BP	V < 200mV	
101	JS2 - 60	ACD_NVETO_05BM	V < 200mV	
102	JS2 - 61	ACD_NVETO_05BP	V < 200mV	
103	JS2 - 62	ACD_NVETO_04BM	V < 200mV	
104	JS2 - 63	ACD_NVETO_04BP	V < 200mV	
105	JS2 - 64	ACD_NVETO_03BM	V < 200mV	
106	JS2 - 65	ACD_NVETO_03BP	V < 200mV	
107	JS2 - 66	ACD_NVETO_02BM	V < 200mV	
108	JS2 - 67	ACD_NVETO_02BP	V < 200mV	
109	JS2 - 68	ACD_NVETO_01BM	V < 200mV	
110	JS2 - 69	ACD_NVETO_01BP	V < 200mV	
111	JS2 - 70	ACD_NVETO_00BM	V < 200mV	
112	JS2 - 71	ACD_NVETO_00BP	V < 200mV	
113	JS2 - 72	ACD_NS DATA_BM	V < 200mV	

114	JS2 - 73	ACD_NSDATA_BP	V < 200mV	
115	JS2 - 74	ACD_NRST_BM	V < 200mV	
116	JS2 - 75	ACD_NRST_BP	V > 2.3V	
117	JS2 - 76	ACD_NSCMD_BM	V < 200mV	
118	JS2 - 77	ACD_NSCMD_BP	V > 2.3V	
119	JS2 - 78	ACD_CLK_BM	1.1V < V < 1.5V	
120	JS2 - 79	ACD_CLK_BP	1.1V < V < 1.5V	

6.2 Electrical Integration of the FREE Card and Initial Current Tests

Verify that all Jumpers installed into breakout boxes. _____

6.3 Measurement of the Power Supply, DC Bias and Reference Voltages

+3.3V Current - _____

+28V Current - _____

Rest of Test Omitted - _____

Meas. No.	FREE Circuit Card Probe Point	Alternate Probe Point	Expected Voltage	Measured Voltage
1	UADC00-5	CA4-1	2.50 V	
2	UADC01-5	C139-1	2.50 V	
3	UADC02-5	C172-1	2.50 V	
4	UADC03-5	C183-1	2.50 V	
5	UADC04-5	C29-1	2.50 V	
6	UADC05-5	C40-1	2.50 V	
7	UADC06-5	C73-1	2.50 V	
8	UADC07-5	C84-1	2.50 V	
9	UADC08-5	C117-1	2.50 V	
10	UADC09-5	C128-1	2.50 V	
11	UADC10-5	C150-1	2.50 V	
12	UADC11-5	C161-1	2.50 V	
13	UADC12-5	C194-1	2.50 V	
14	UADC13-5	C208-1	2.50 V	
15	UADC14-5	C51-1	2.50 V	
16	UADC15-5	C62-1	2.50 V	
17	UADC16-5	C95-1	2.50 V	
18	UADC17-5	C106-1	2.50 V	
19	UGA00-8	C266-1	2.50 V	
20	UGA01-8	C248-1	2.50 V	
21	UGA02-8	C257-1	2.50 V	
22	UGA03-8	C260-1	2.50 V	
23	UGA04-8	C218-1	2.50 V	
24	UGA05-8	C221-1	2.50 V	
25	UGA06-8	C230-1	2.50 V	
26	UGA07-8	C233-1	2.50 V	
27	UGA08-8	C242-1	2.50 V	

28	UGA09-8	C245-1	2.50 V	
29	UGA10-8	C251-1	2.50 V	
30	UGA11-8	C254-1	2.50 V	
31	UGA12-8	C263-1	2.50 V	
32	UGA13-8	C269-1	2.50 V	
33	UGA14-8	C224-1	2.50 V	
34	UGA15-8	C227-1	2.50 V	
35	UGA16-8	C236-1	2.50 V	
36	UGA17-8	C239-1	2.50 V	
37	UGA00-22 (VDD)	CA5-1	> 3.1 V	
38	UGA01-22 (VDD)	CA5-1	> 3.1 V	
39	UGA02-22 (VDD)	C143-1	> 3.1 V	
40	UGA03-22 (VDD)	C176-1	> 3.1 V	
41	UGA04-22 (VDD)	C33-1	> 3.1 V	
42	UGA05-22 (VDD)	C44-1	> 3.1 V	
43	UGA06-22 (VDD)	C77-1	> 3.1 V	
44	UGA07-22 (VDD)	C88-1	> 3.1 V	
45	UGA08-22 (VDD)	C121-1	> 3.1 V	
46	UGA09-22 (VDD)	C132-1	> 3.1 V	
47	UGA10-22 (VDD)	C154-1	> 3.1 V	
48	UGA11-22 (VDD)	C165-1	> 3.1 V	
49	UGA12-22 (VDD)	C198-1	> 3.1 V	
50	UGA13-22 (VDD)	C212-1	> 3.1 V	
51	UGA14-22 (VDD)	C55-1	> 3.1 V	
52	UGA15-22 (VDD)	C66-1	> 3.1 V	
53	UGA16-22 (VDD)	C99-1	> 3.1 V	
54	UGA17-22 (VDD)	C110-1	> 3.1 V	
55	UGA00-1 (VCC)	CA7-1	> 3.1 V	
56	UGA01-1 (VCC)	C145-1	> 3.1 V	
57	UGA02-1 (VCC)	C178-1	> 3.1 V	
58	UGA03-1 (VCC)	C189-1	> 3.1 V	
59	UGA04-1 (VCC)	C35-1	> 3.1 V	
60	UGA05-1 (VCC)	C46-1	> 3.1 V	
61	UGA06-1 (VCC)	C79-1	> 3.1 V	
62	UGA07-1 (VCC)	C90-1	> 3.1 V	
63	UGA08-1 (VCC)	C123-1	> 3.1 V	
64	UGA09-1 (VCC)	C134-1	> 3.1 V	
65	UGA10-1 (VCC)	C156-1	> 3.1 V	
66	UGA11-1 (VCC)	C167-1	> 3.1 V	
67	UGA12-1 (VCC)	C200-1	> 3.1 V	
68	UGA13-1 (VCC)	C214-1	> 3.1 V	
69	UGA14-1 (VCC)	C57-1	> 3.1 V	
70	UGA15-1 (VCC)	C68-1	> 3.1 V	
71	UGA16-1 (VCC)	C101-1	> 3.1 V	
72	UGA17-1 (VCC)	C112-1	> 3.1 V	
73	TPR1	UR1-2	< 0.2 V	
74	DR1-A	UR1-1	> 3.0 V	
75	UID1-1	N/A	< 0.2 V	
76	UID1-2	N/A	< 0.2 V	
77	UID1-3	N/A	N/A (ID_4)	
78	UID1-4	N/A	N/A (ID_5)	

79	UID1-5	N/A	N/A (ID_6)	
80	UID1-6	N/A	N/A (ID_7)	
81	UID1-11	N/A	N/A (ID_0)	
82	UID1-12	N/A	N/A (ID_1)	
83	UID1-13	N/A	N/A (ID_2)	
84	UID1-14	N/A	N/A (ID_3)	

6.4 Measurement of the GARC Bias Resistors and Voltages

Test Omitted - _____

FREE Resistor	Value	Measured	Recorded from FREE Assembly Documentation
RG1			
RG2			
RG3			
RG4			
RG5			
RG6			
RG7			
RG8			
RG9			
RG10			

GARC Bias Signal	GARC Pin	Resistor Test Point	Expected Voltage (+/- 0.1 V)	Measured Voltage
HLD_WOR_BIAS	104	RG8	1.64	
BIAS_RCVR	156	RG6	1.10	
BIAS_DRV_H	160	RG3	1.53	
BIAS_DRV_L	169	RG1	1.75	
LVDS_PRESET_ADJ	184	RG9	1.52	

6.5 Verification of the Power on Reset Pulse

Reset Pulse Width verified - _____ (100 – 200mSec)

6.6 Measurement of the Power Supply Quality at the ACD Interface

Test Omitted - _____

Meas. No.	Signal Name	FREE Circuit Card Break Out Box V+ Probe	FREE Circuit Card Break Out Box RTN Probe	Measured DC Voltage	Expected DC Voltage	Measured RMS Voltage	Expected RMS Voltage
1	+3.3 V Primary	JP1-1	JP1-30		3.20 – 3.60		< 5 mV RMS
2	+28 V Primary	JP1-5	JP1-33		22.0 – 38.7		< 10 mV RMS
3	+3.3V Secondary	JS2-1	JS2-30		3.20 – 3.60		< 5 mV RMS
4	+28 V Secondary	JS2-5	JS2-33		22.0 – 38.7		< 10 mV RMS

7.1 GARC and GAFE Registers Initial Reset Test

Turn On reset verified - _____

FREE Board ID - _____

Reset Command verified - _____

8.1 FREE Power Measurement at the Nominal Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.3V Current Measured (mA)	+3.3V Current Expected (mA)
LVDS “A” Drivers Enabled			
LVDS “B” Drivers Enabled	768		200 ± 10mA
LVDS “A” Drivers Enabled			
LVDS “B” Drivers Disabled	256		150 ± 10mA
LVDS “A” Drivers Disabled			
LVDS “B” Drivers Enabled	512		150 ± 10mA
LVDS “A” Drivers Disabled			
LVDS “B” Drivers Disabled	0		95 ± 10mA

8.2 FREE Power Measurement at the Minimum Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.0V Current Measured (mA)	+3.0V Current Expected (mA)
LVDS “A” Drivers Enabled			
LVDS “B” Drivers Enabled	768		170 ± 10mA
LVDS “A” Drivers Enabled			
LVDS “B” Drivers Disabled	256		125 ± 10mA

LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		$125 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		$75 \pm 10\text{mA}$

8.3 FREE Power Measurement at the Maximum Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.6V Current Measured (mA)	+3.6V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		$230 \pm 10\text{mA}$
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		$175 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		$175 \pm 10\text{mA}$
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		$115 \pm 10\text{mA}$

8.4 GARC/GAFE Register Read/Write Tests

This test may be automated using the LabView GSE via the [Register Test VI](#).

Test Completed - _____

8.44 Initial GAFE Logic Reset Test

This test may be automated using the LabView GSE via the [GAFE Logic Reset Test.txt](#) script.

Test Completed - _____

8.45 GAFE ASIC Broadcast Command Functional Verification

This test may be automated using the LabView GSE via the [GAFE Broadcast Command Test.txt](#) script.

Test Completed - _____

8.46 Test of the GARC Parity Test

This test may be automated using the LabView GSE via the [GARC Parity Test.txt](#) script.

Test Completed - _____

8.47 Test of the Look-At-Me Circuitry

This test may be automated using the LabView GSE via the [GARC Look At Me Test.txt](#) script.

Test Completed - _____

8.48 Maximum PHA Return Test

This test may be automated using the LabView GSE via the GARC Max PHA Return Test.tst script.

Test Completed - _____

8.49 PHA Enable/Disable Test

This test may be automated using the LabView GSE via the GARC PHA Enable Test.tst script.

Test Completed - _____

8.50 PHA Threshold Verification Test

This test may be automated using the LabView GSE via the GARC PHA Threshold Test.txt script.

Test Completed - _____

8.51 Data Phase Command Test

Test Omitted - _____

Test Completed - _____

9.1 HVBS Connector Checks and Circuit Check-Outs

Test Omitted - _____

Meas. No.	FREE Circuit Card Probe Point	Expected Voltage (+/- 50 mV)	Measured Voltage
1	TPREF1	1.25V	
2	TPDAC2	0V	
3	JDAC2	1.40V	
4	TPDAC3	2.50V	
5	JDAC1	0V	
6	TPDAC4	0V	
7	UDAC1D-14 (VREF)	2.50V	
8	JHV1-4 (HV-DACP)	1.40V	
9	JHV1-9 (HV-DACN)	1.40V	

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script.

Meas. No.	DAC SETTING	JHV1-4 (HV-DACP)	JHV1-9 (HV-DACN)	JDAC1 (DAC VOLTAGE)
1	0			
2	200			
3	400			
4	600			
5	800			
6	1000			
7	1200			
8	1400			
9	1600			
10	1800			
11	2000			
12	2200			
13	2400			
14	2600			
15	2800			
16	3000			
17	3200			
18	3400			
19	3600			
20	3800			
21	4000			
22	4095			

9.2 Test of the HVBS Triple Modular Redundancy Circuitry

This test may be automated using the LabView GSE via the GARC HV Enable Test.tst script.

Voltage at JHV1-5 when Enabled - _____ (3.7V)

Voltage at JHV2-5 when Enabled - _____ (3.7V)

Voltage at JHV1-5 when Disabled - _____ (0.04V)

Voltage at JHV2-5 when Disabled - _____ (0.04V)

Test Completed - _____

9.3 Capture of the DAC Control Signals

Test Omitted - _____

Send HVNormal 2650

Record NDAC_CS (RDA21) pulse width - _____(3.2uSec)

Record DAC Clock (RDA31) Frequency - _____ (5Mhz)

DAC_DATA (RDA30) and DAC_ReadBack (RDA26) Pulses Verified - _____

Record Reset Pulse (RDA24) Width - _____(150nSec)

9.4 TEST OF THE SAA/HV NORMAL MODES

Set HVBS Normal to 2048 and SAA to 1024

3. Using a multimeter at the JHV1 pin 4 connector, verify the HV_DACP voltage is 1.4V

Value observed: _____

4. Send the Use_HV_Nominal command. Verify that the HV_DACP voltage is 2.1V.

Value observed: _____

5. Send the DAC_HVReg_Rd command and verify the return data pattern from the MAX5121 DAC is decimal 10240.

Value observed: _____

6. Send the Use_SAA_Level command. Verify that the HV_DACP voltage is 1.8V.

Value observed: _____

7. Send the DAC_SAAReg_Rd command and verify the return data pattern from the MAX5121 DAC is decimal 9216.

Value observed: _____

8. Send the GARC_Reset command. Verify that the HV_DACP voltage is 1.4V..

Value observed: _____

10.0 Characterizations of the FREE Assembly In-Rush Currents

Test Omitted - _____

Printout of the waveforms attached - _____

11.1 GARC Test Pin Mux Verification

Test Omitted - _____

4. Send the GARC_Mode_Wr command with a data argument of 1792 for “Live” mode. Verify the signal at (TP179).
5. Send the GARC_Mode_Wr command with a data argument of 768 for “Hitmap” mode. Verify the signal (TP179).

Test Completed - _____

11.2 Test of the Hold Delay Operation

Test Omitted - _____

GAFE_HOLD_P (RT3) Voltage - _____ (870mV)

GAFE_HOLD_M (RT3) Voltage - _____ (1600mV)

The LabView test script **GARC Hold Delay Test.tst** may be used to partially automate this test. Monitor HLD at JHLD0, and trigger on Trig_TST at TP180.

Test Completed - _____

11.4 Veto Delay Test

This test may be automated using the LabView GSE via the script **GARC VETO Delay Test.tst**. Capture and attach a copy of the waveforms showing the Tail pulse and the Veto signal for one of the channels.

Test Completed - _____

11.5 Veto Width Test

The setup for this test is the same as the VETO Delay test above. This test may be automated using the LabView GSE via the **GARC VETO Width Test.tst** script.

Test Completed - _____

11.6 Veto Enable and Disable Test

This test may be automated when using the LabView GSE via test script **GARC VETO Disable A/B Side Test.tst**. Monitor the counters to verify the Veto signals.

1. Send the GARC_Mode_Wr command with the value of 768 to enable the “A” and enable the “B” side VETOs.

JP1-71 - _____ (expected 400mV)

JS2-71 - _____ (expected 400mV)

2. Send the GARC_Mode_Wr command with the value of 512 to disable the “A” and enable the “B” side VETOs.

JP1-71 - _____ (expected 50mV)

JS2-71 - _____ (expected 400mV)

3. Send the GARC_Mode_Wr command with the value of 256 to enable the “A” and disable the “B” side VETOs.

JP1-71 - _____ (expected 400mV)

JS2-71 - _____ (expected 50mV)

4. Send the GARC_Mode_Wr command with the value of 0 to disable both the “A” and “B” side VETOs.

JP1-71 - _____ (expected 50mV)

JS2-71 - _____ (expected 50mV)

Side A Test Completed - _____

Side B Test Completed - _____

11.8 HitMap Width Test

Test Omitted - _____

This test may be automated using the LabView GSE via the [GARC HitMap Width Test.tst](#) script.
Monitor TP179.

Test Completed - _____

11.9 HitMap Delay Test

Test Omitted - _____

This test may be automated using the LabView GSE via the [GARC HitMap Delay Test.tst](#) script.

Test Completed - _____

11.10 HitMap Deadtime Stretch Test

Test Omitted - _____

This test may be automated using the LabView GSE via [the GARC HitMap Deadtime Test.tst](#) script.

Test Completed - _____

11.11 Strobe Test

Test Omitted - _____

Measure the DC levels of both STROBE_P and STROBE_M and record the values below, monitor the Live signal at TP179.

STROBE_P (RT4) (DC): _____ (expected ~ 700 mV)

STROBE_M (RT4) (DC): _____ (expected ~ 1600 mV)

STROBEP to STROBEM differential voltage: _____ (expected 900 mV)

Live-to-STROBE delay: _____ (expected ~ 150 ns)

STROBE pulse duration (μsec): _____ (expected 12.5 μsec)

11.12 Capture of the ADC Control Signals

Test Omitted - _____

Clock (RA3) rate measured: _____ MHz

Chip Select Duration (RA6) _____ (expected ~ 10.6 μsec)

11.13 ADC TACQ Test

This test may be automated using the LabView GSE script [GARC ADC TACQ Test.tst](#). Monitor ADC Clock (RA3) and Chip Select (RA6).

Test Completed - _____

11.14 Test of the GARC LVDS Circuitry Driver Currents

Test Omitted - _____

Obtain a scope picture of the nominal pulse Amplitude Swings

GARC Signal	Signal Location	- DC Level (V) Enabled	+ DC Level (V) Disabled	- DC Level (V) Enabled	+ DC Level (V) Disabled
ACD_NVETO_12B	R1				
ACD_NVETO_12A	R2				
ACD_NVETO_11B	R3				
ACD_NVETO_11A	R4				
ACD_NVETO_10B	R5				
ACD_NVETO_10A	R6				
ACD_NVETO_09B	R7				
ACD_NVETO_09A	R8				
ACD_NVETO_08B	R9				
ACD_NVETO_08A	R10				
ACD_NVETO_07B	R11				
ACD_NVETO_07A	R12				
ACD_NVETO_06B	R13				
ACD_NVETO_06A	R14				

ACD_NVETO_05B	R15				
ACD_NVETO_05A	R16				
ACD_NVETO_04B	R17				
ACD_NVETO_04A	R18				
ACD_NVETO_03B	R19				
ACD_NVETO_03A	R20				
ACD_NVETO_02B	R21				
ACD_NVETO_02A	R22				
ACD_NVETO_01B	R23				
ACD_NVETO_01A	R24				
ACD_NVETO_00B	R25				
ACD_NVETO_00A	R26				
ACD_CNO_B	R27				
ACD_CNO_A	R28				
ACD_NVETO_13B	R31				
ACD_NVETO_13A	R32				
ACD_NVETO_14B	R33				
ACD_NVETO_14A	R34				
ACD_NVETO_15B	R35				
ACD_NVETO_15A	R36				
ACD_NVETO_16B	R37				
ACD_NVETO_16A	R38				
ACD_NVETO_17B	R39				
ACD_NVETO_17A	R40				
ACD_NSDATA_B	R29				
ACD_NSDATA_A	R30				

Measure the GAFE to GARC LVDS signals.

Obtain a scope picture of the nominal pulse Amplitude Swings

Test Omitted - _____

GARC Signal	GAFE "n" Pin	DC Level (V)	Switch Swing (V)
DISC_00	26		
CHID_00	25		
IRTN_00	24		
DISC_01	26		
CHID_01	25		
IRTN_01	24		
DISC_02	26		
CHID_02	25		
IRTN_02	24		
DISC_03	26		
CHID_03	25		
IRTN_03	24		
DISC_04	26		
CHID_04	25		
IRTN_04	24		
DISC_05	26		
CHID_05	25		
IRTN_05	24		
DISC_06	26		
CHID_06	25		
IRTN_06	24		

DISC 07	26		
CHID 07	25		
IRTN 07	24		
DISC 08	26		
CHID 08	25		
IRTN 08	24		
DISC 09	26		
CHID 09	25		
IRTN 09	24		
DISC 10	26		
CHID 10	25		
IRTN 10	24		
DISC 11	26		
CHID 11	25		
IRTN 11	24		
DISC 12	26		
CHID 12	25		
IRTN 12	24		
DISC 13	26		
CHID 13	25		
IRTN 13	24		
DISC 14	26		
CHID 14	25		
IRTN 14	24		
DISC 15	26		
CHID 15	25		
IRTN 15	24		
DISC 16	26		
CHID 16	25		
IRTN 16	24		
DISC 17	26		
CHID 17	25		
IRTN 17	24		

12.1 FREE Circuit Assembly Characterization Tests

Characterization of each of the 18 GAFE chips

Run script _____

Data file used: _____

All printouts are to be attached to the Test Results Record.

Settings to be used based on the characterization test:

Create a configuration script for the FREE board under test.

File Name _____

GAFE Configuration

GAFE Channel	Mode	VETO DAC	VETO VERNIER	HLD DAC	BIAS DAC	TCI DAC
0						
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						

GARC Configuration

Register	Test Value
Veto_Delay	
HVBS_Level	
SAA_Level	
Hold_Delay	
Veto_Width	
HitMap_Width	
HitMap_Deadtime	
HitMap_Delay	
PHA_En0	
PHA_En1	
VETO_En0	
VETO_En1	
Max_PHA	

GARC_Mode	
FREE_Board_ID	
GARC_Version	
PHA_Threshold_00	
PHA_Threshold_01	
PHA_Threshold_02	
PHA_Threshold_03	
PHA_Threshold_04	
PHA_Threshold_05	
PHA_Threshold_06	
PHA_Threshold_07	
PHA_Threshold_08	
PHA_Threshold_09	
PHA_Threshold_10	
PHA_Threshold_11	
PHA_Threshold_12	
PHA_Threshold_13	
PHA_Threshold_14	
PHA_Threshold_15	
PHA_Threshold_16	
PHA_Threshold_17	
ADC_TACQ	

12.2 MUXSH DC Level and Pedestal Check

Test Omitted - _____

PHA RANGE MODE bit = 1 (Auto Ranging off) and the RANGE SELECT bit = 0 (Low Range).

GAFE Channel	BIAS 0 Low Range	BIAS 0 High Range	BIAS 2 Low Range	BIAS 2 High Range	BIAS 4 Low Range	BIAS 4 High Range	BIAS 6 Low Range	BIAS 6 High Range
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								

10								
11								
12								
13								
14								
15								
16								
17								

12.3 VETO and ADC Crosstalk Test

Test Omitted - _____

Disconnect the pulser from the Ct Box.

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

Data file used: _____

GAFE Channel	Crosstalk Checked	Single VETO Verified
0		
1		
2		
3		
4		
5		
6		
7		

8		
9		
10		
11		
12		
13		
14		
15		
16		
17		

12.4 Multiple System Clock Speed Test

Test Omitted - _____

+3.0V current - _____

Clock Frequency set to 22MHz

Register Test Complete - _____

DAC Checkout. This test may be automated using the LabView GSE via the [GARC HVBS DAC Level Test.txt](#) script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

Baseline Checkout

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

13	
14	
15	
16	
17	

Data file used: _____

+3.6V current - _____

Register Test Complete - _____
 DAC Checkout. This test may be automated using the LabView GSE via the **GARC HVBS DAC Level Test.txt** script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

Baseline Checkout

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

Data file used: _____

Clock Frequency set to 14MHz

Register Test Complete - _____

DAC Checkout. This test may be automated using the LabView GSE via the [**GARC HVBS DAC Level Test.txt**](#) script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

Baseline Checkout

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

Data file used: _____

Set the power supply to +3.0V.

Register Test Complete - _____

DAC Checkout. This test may be automated using the LabView GSE via the [**GARC HVBS DAC Level Test.txt**](#) script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

Baseline Checkout

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

Data file used: _____

12.5 Power Supply Rail Tests – 3.0V to 3.6V

Test Omitted - _____

Voltage set to 3.6V

Characterization of each of the 18 GAFE chips

Data file used: _____

All printouts are to be attached to the Test Results Record.

Voltage set to 3.0V

Characterization of each of the 18 GAFE chips

Data file used: _____

All printouts are to be attached to the Test Results Record.

12.6 Differential Non-Linearity (DNL) Test

Test Omitted - _____

Data file used: _____

Test Completed - _____

END OF COMPREHENSIVE PERFORMANCE TEST